“Method for Joining Conductive Structures
and an Electrical Conductive Article”
Inventors: Kuo-Chuan Liu, et al.
Application Serial No.: 10/066,485

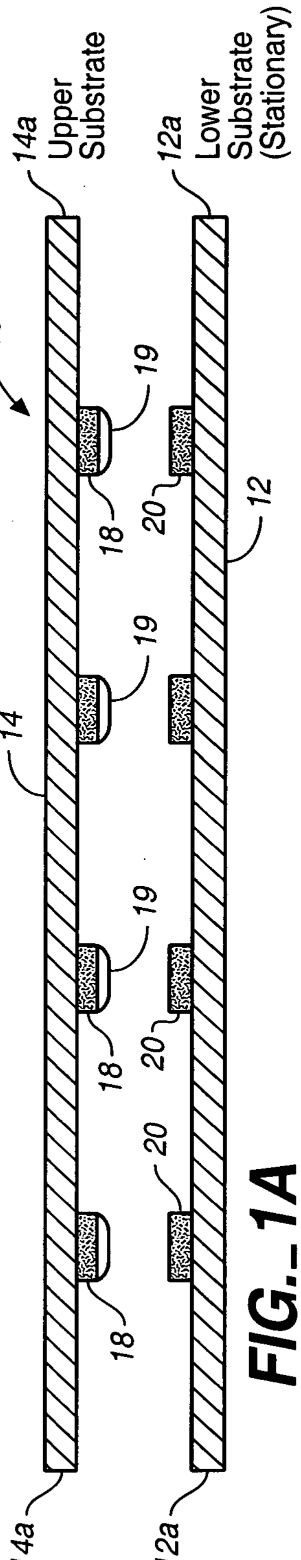


FIG._1A

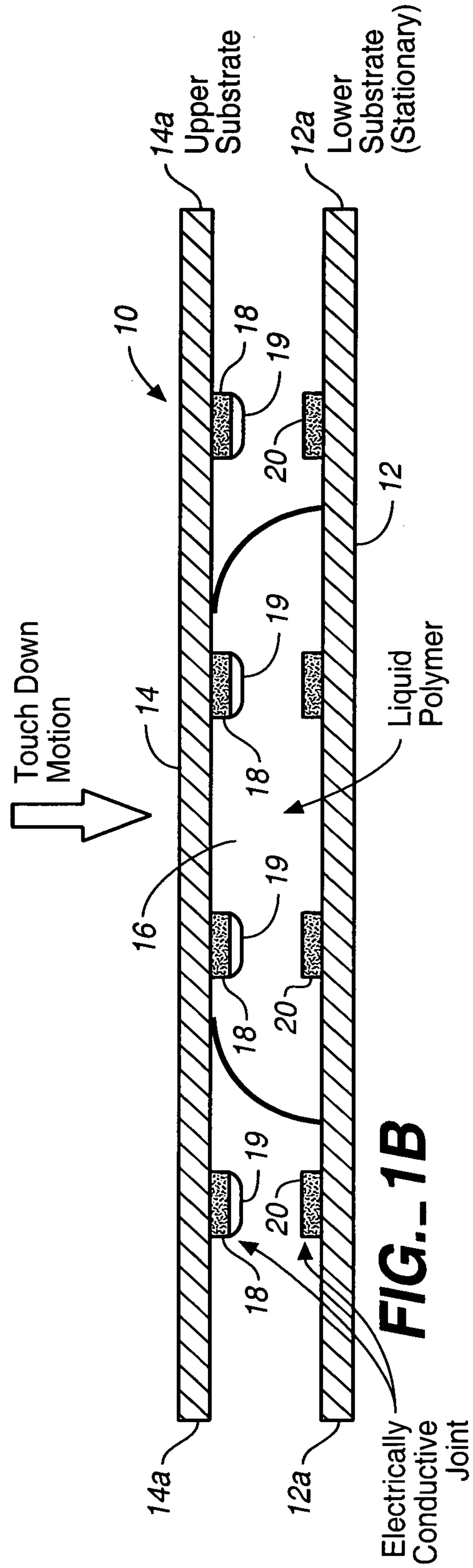


FIG._1B

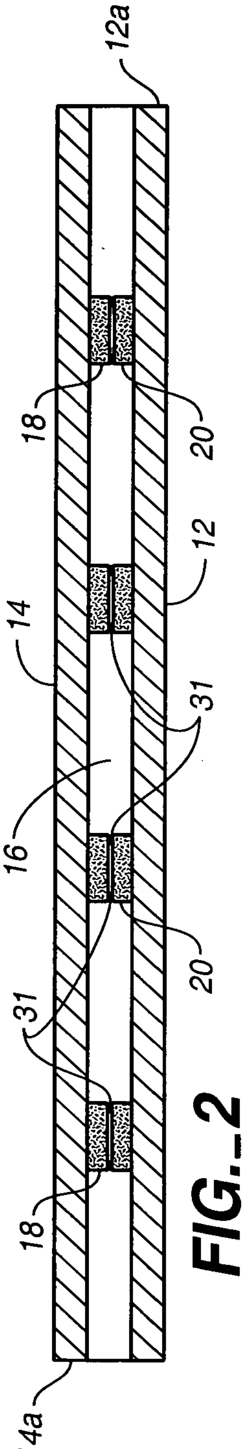


FIG._2

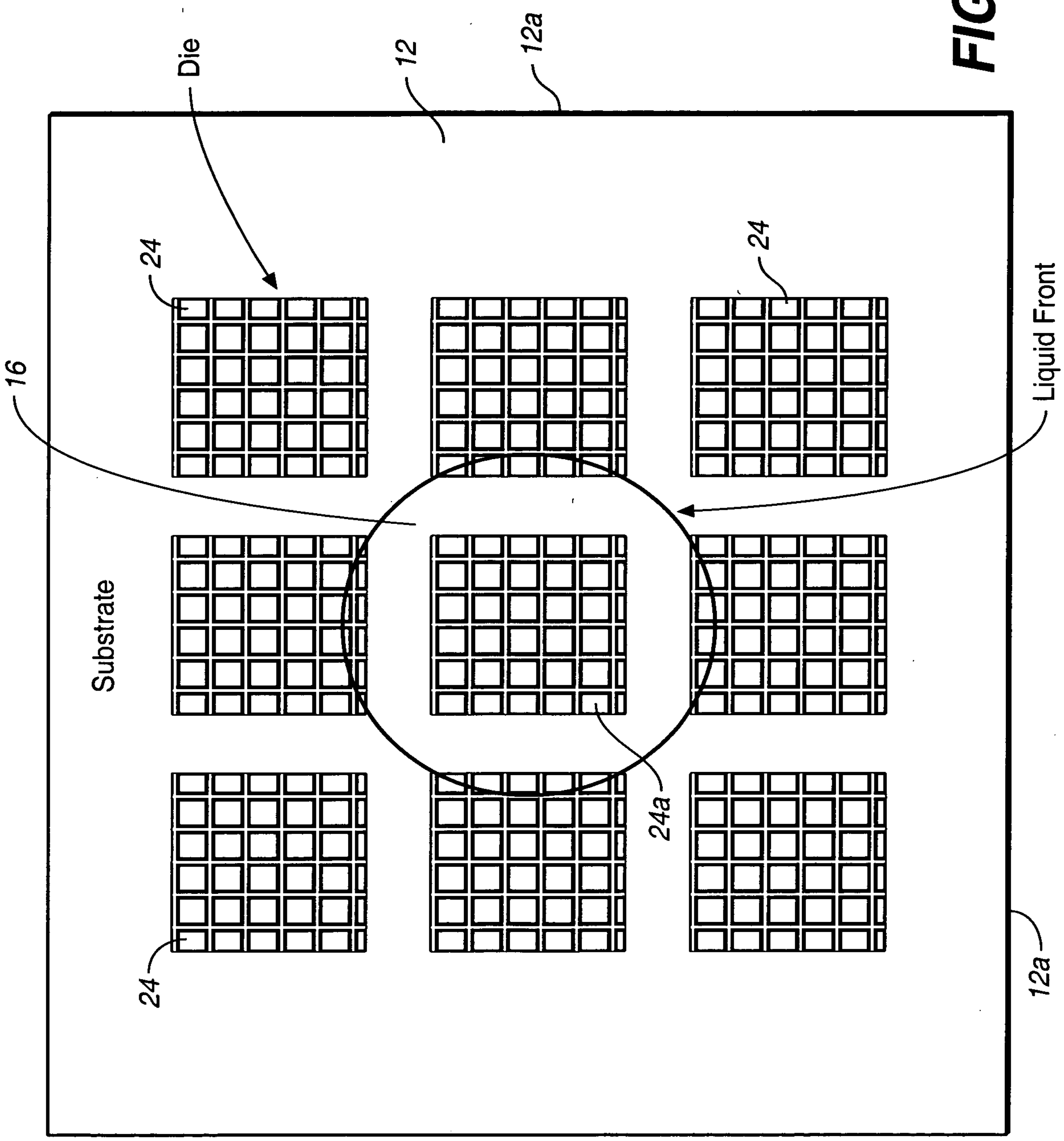


FIG._3

FIG._4

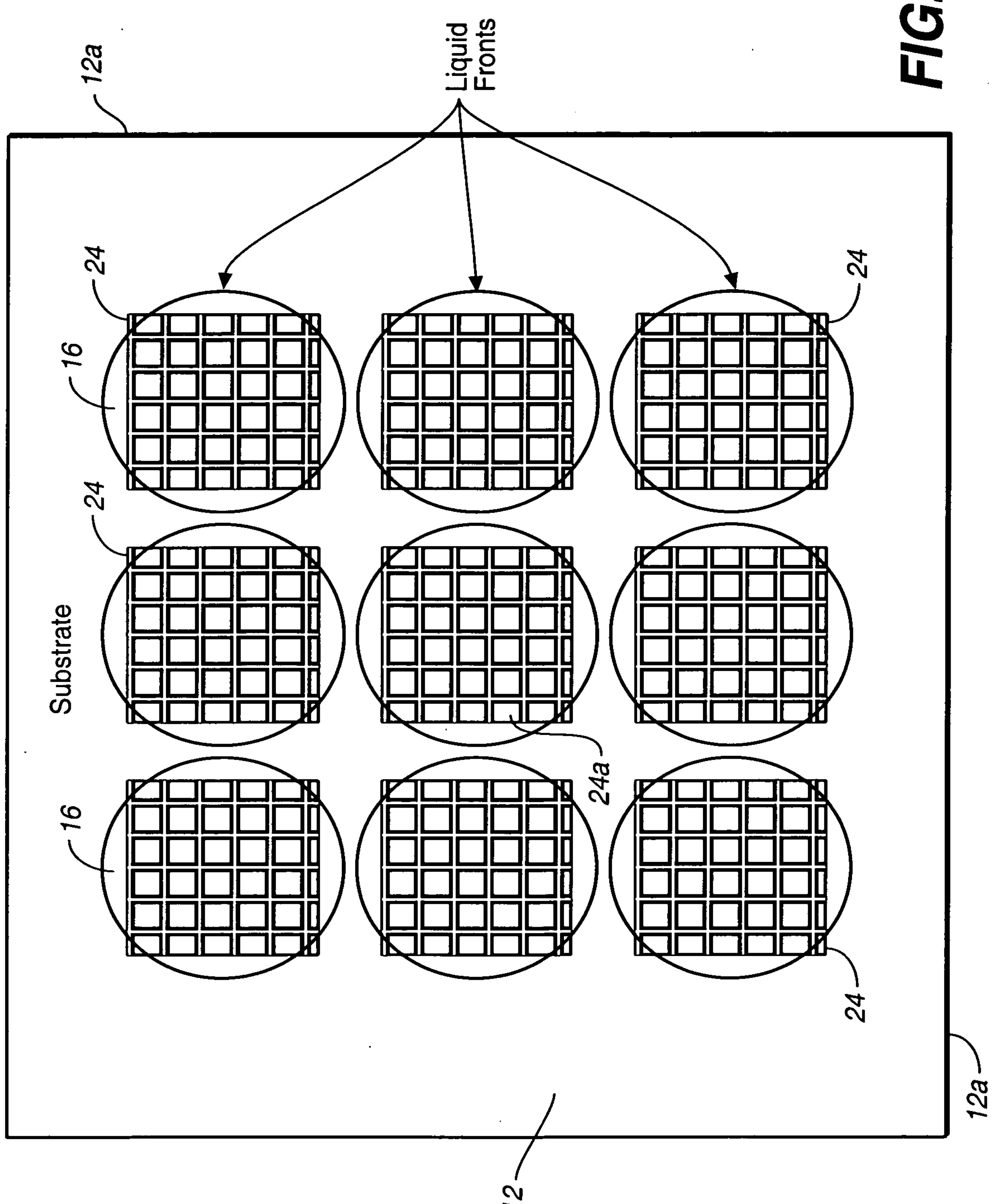
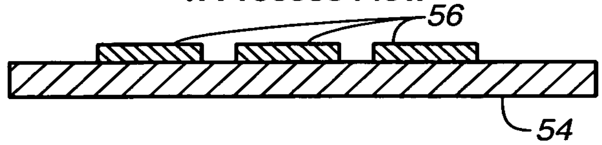


FIG._5

1. Process Flow

1

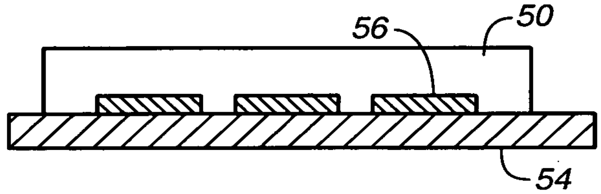


L / D Preparation

FIG._6

2. Process Flow

2

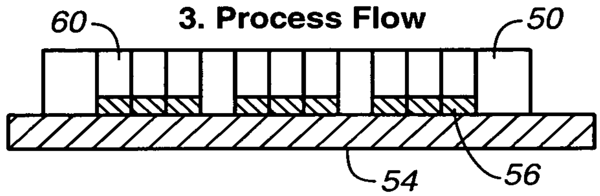


Bonding Sheet
Tack Lam

FIG._7

3. Process Flow

3

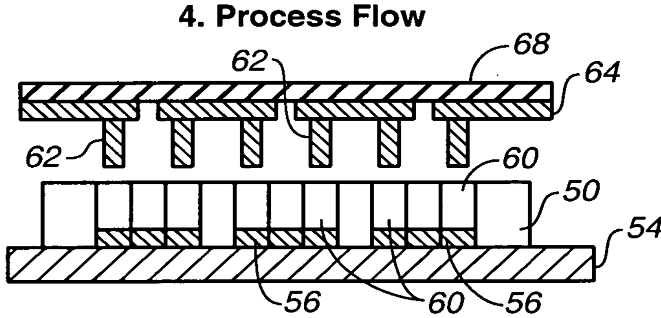


Laser Drill of
Lithography

FIG._8

4. Process Flow

4

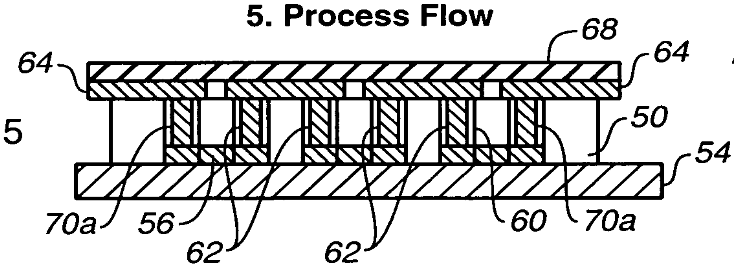


Align DDF
to L / D

FIG._9

5. Process Flow

5

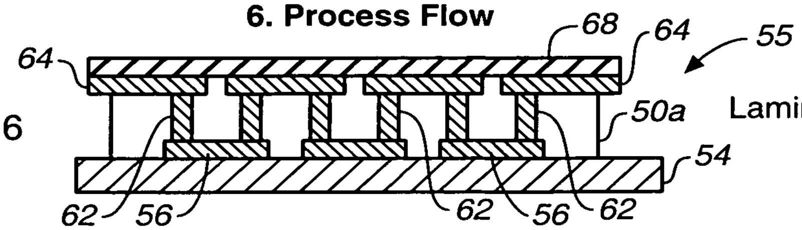


Attach DDF
to L / D
by Heat

FIG._10

6. Process Flow

6



Lamination

The Concept

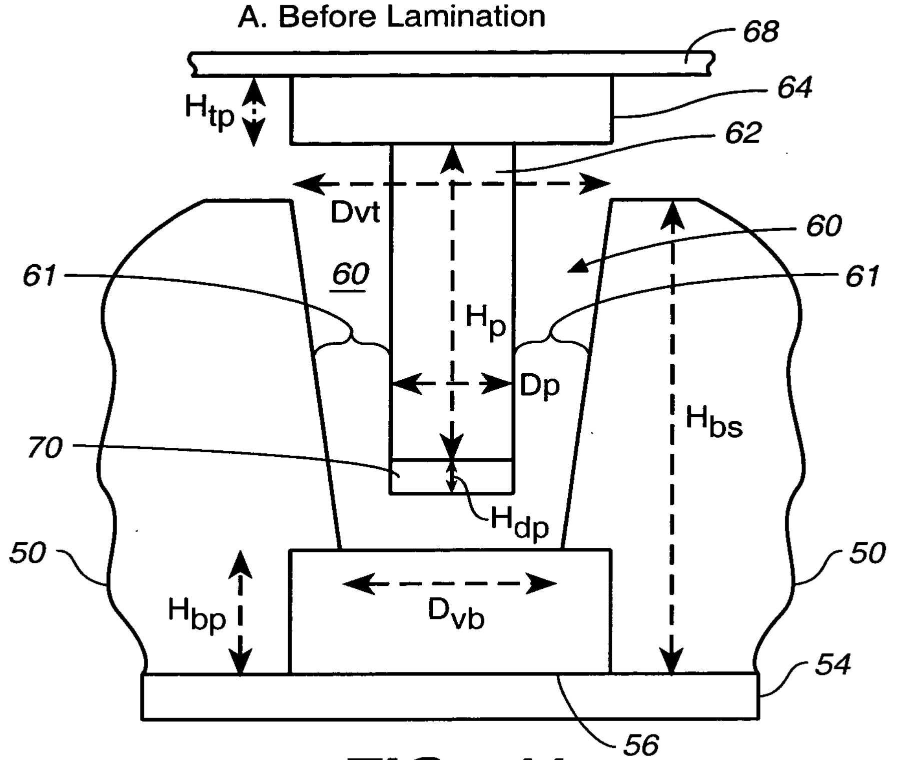


FIG._11

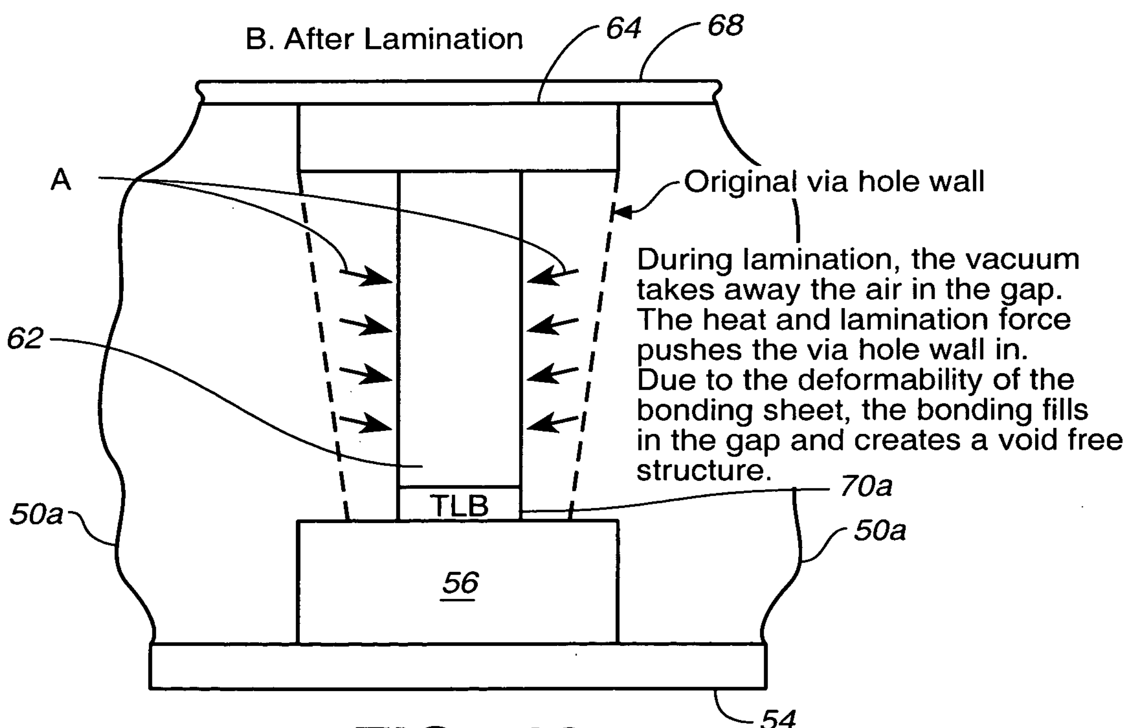


FIG._12

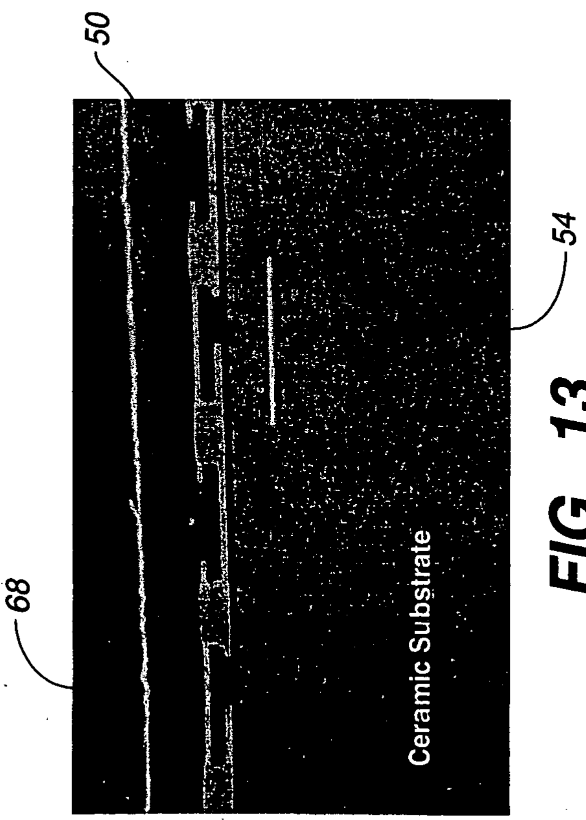


FIG._13

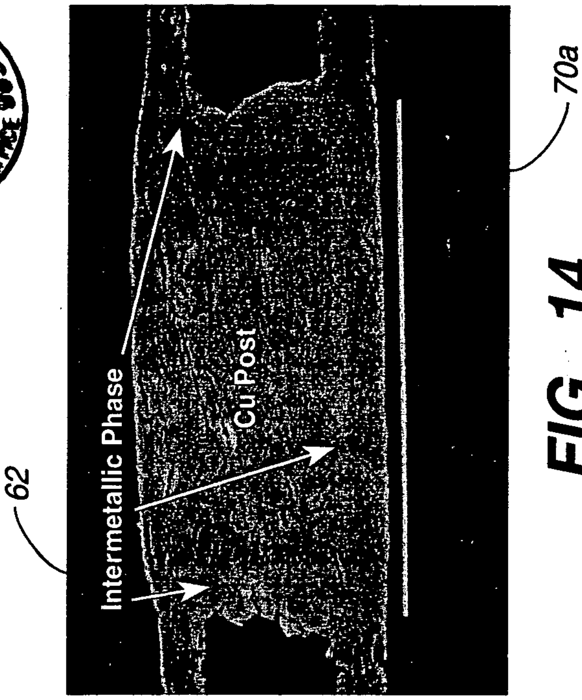


FIG._14

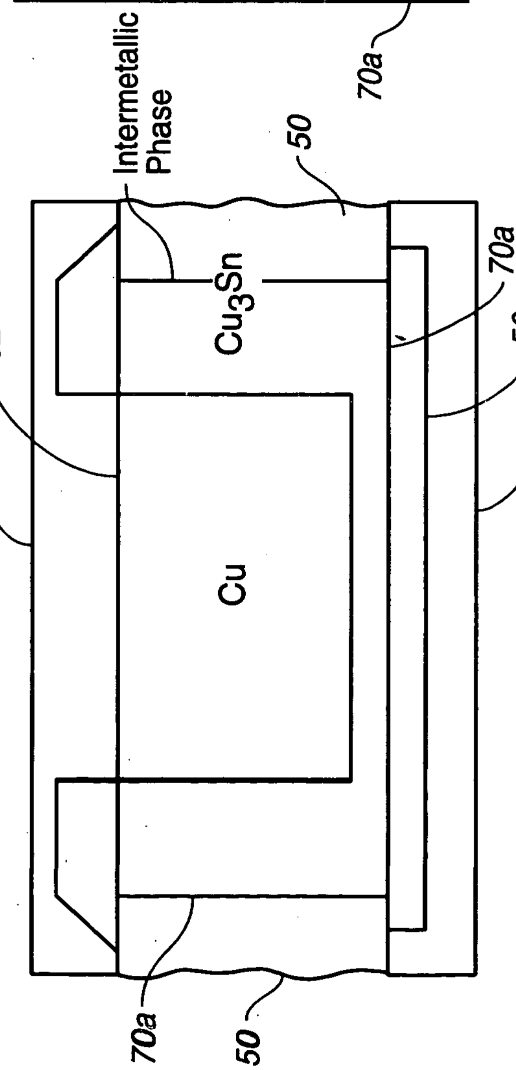


FIG._15

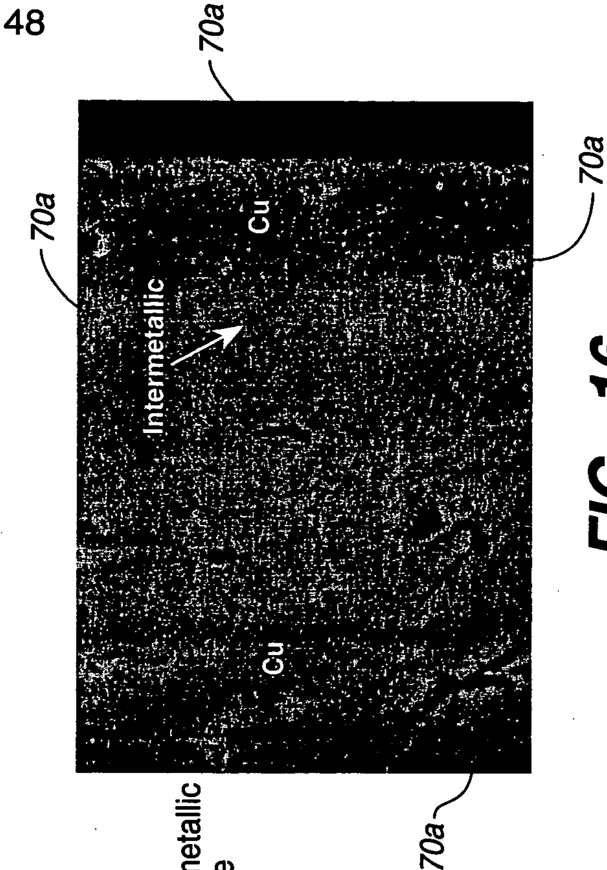
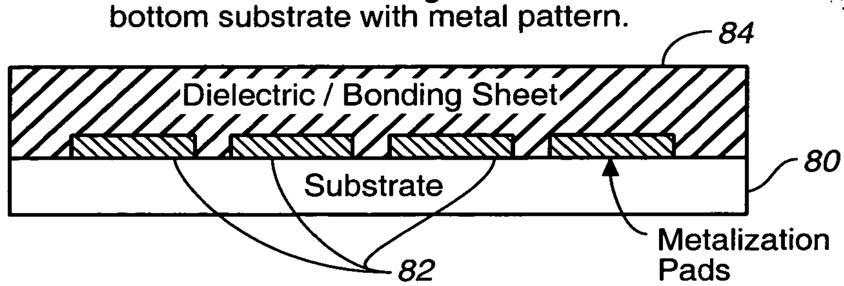


FIG._16

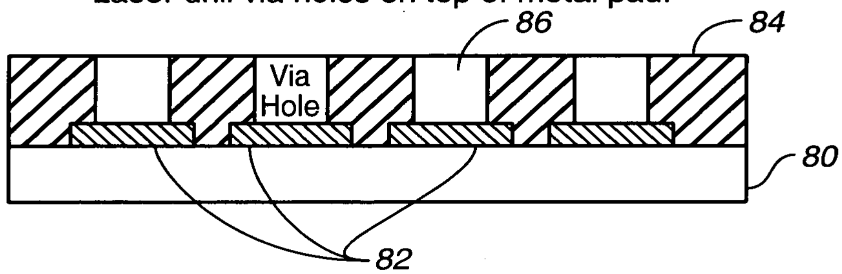
Tack lam the bonding sheet onto bottom substrate with metal pattern.

FIG._17



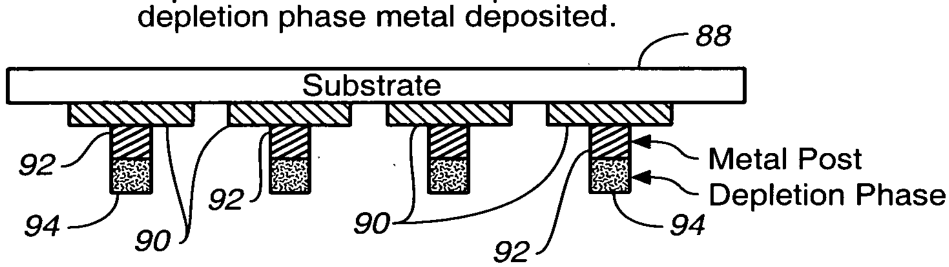
Laser drill via holes on top of metal pad.

FIG._18



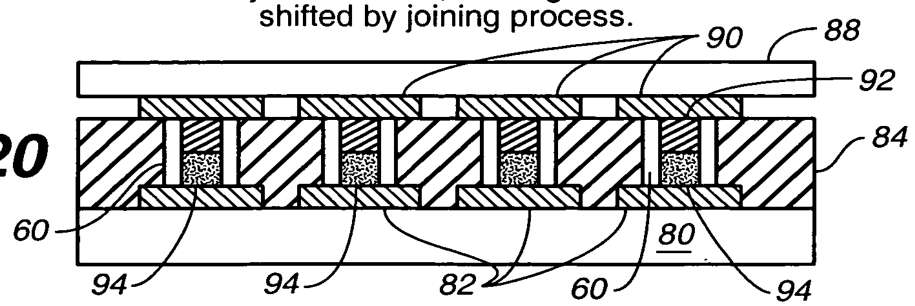
Top substrate has metal post and depletion phase metal deposited.

FIG._19



Top substrate is aligned to the holes on bottom substrate and laminated under pressure, temperature and in certain period of time. Because the post is anchored by the via hole, the alignment will not be shifted by joining process.

FIG._20



After lamination at suitable temperature for both bonding sheet and Transient Liquid Alloy Joints, the final structure has a filled via with metal post embedded inside intermetallic wall.

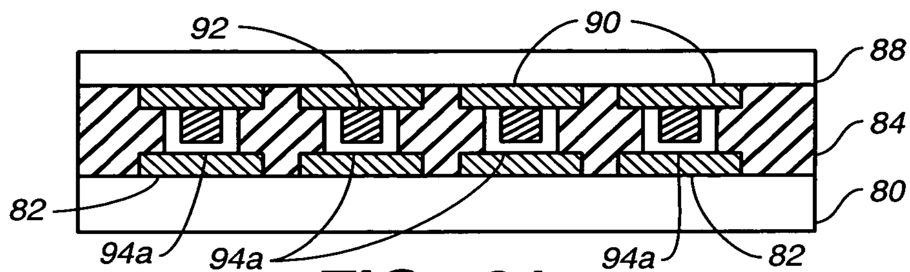


FIG._21

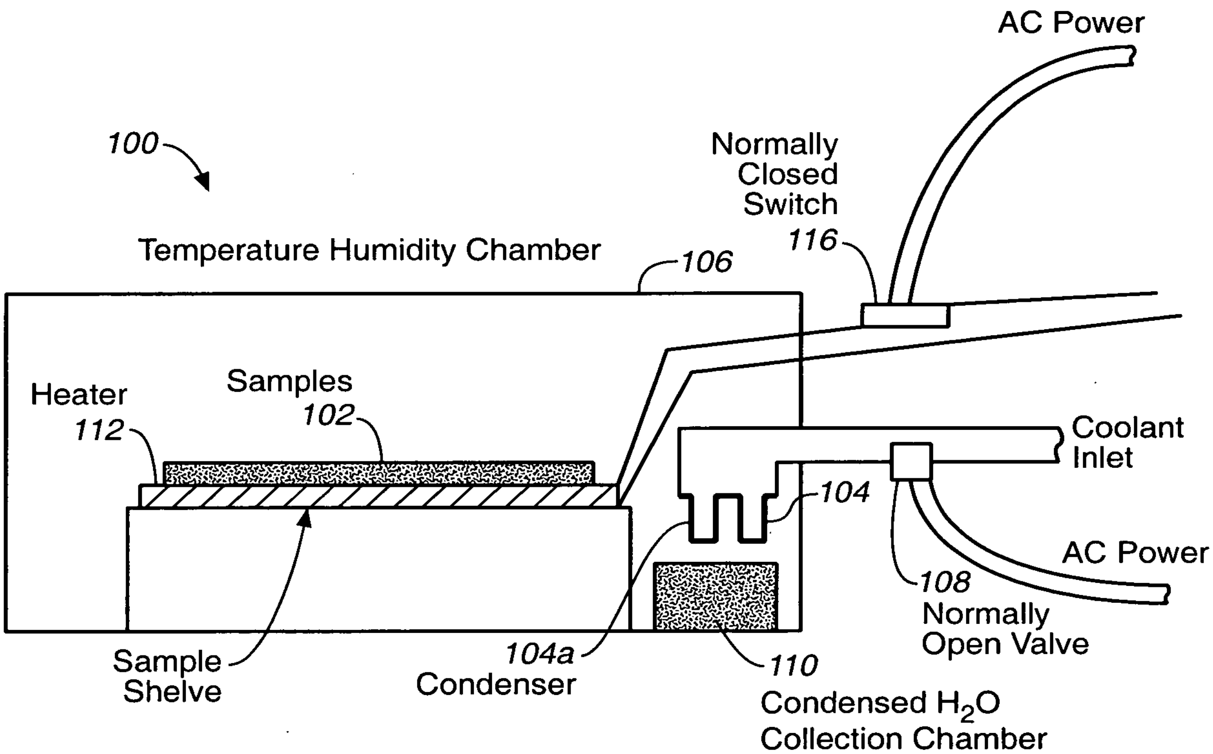
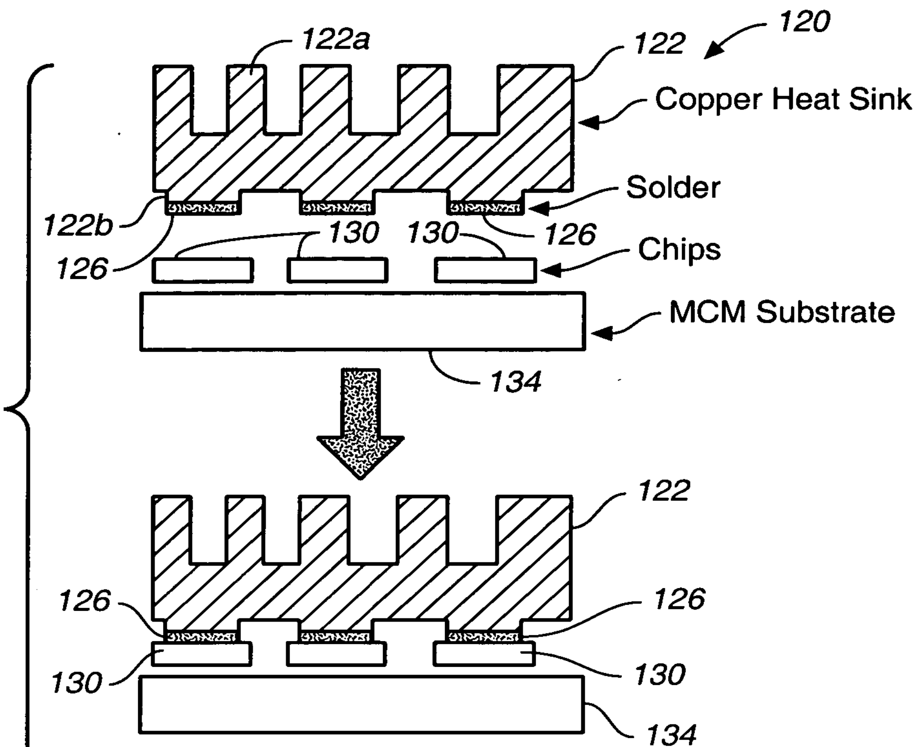


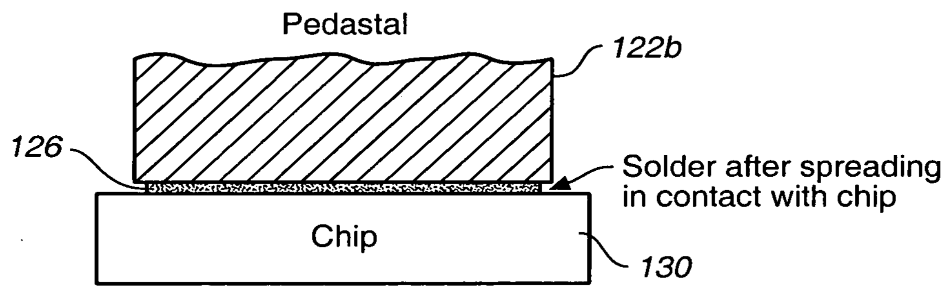
FIG._22

FIG._23



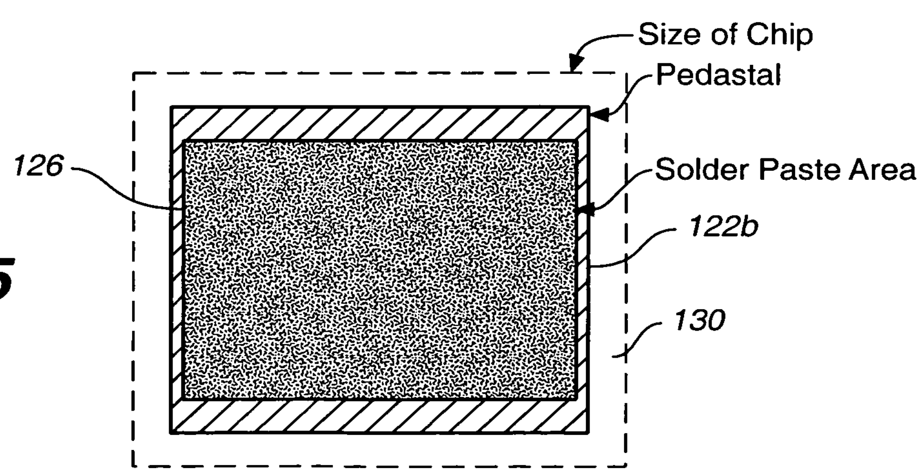
1. Illustration depicting general concept

FIG._24



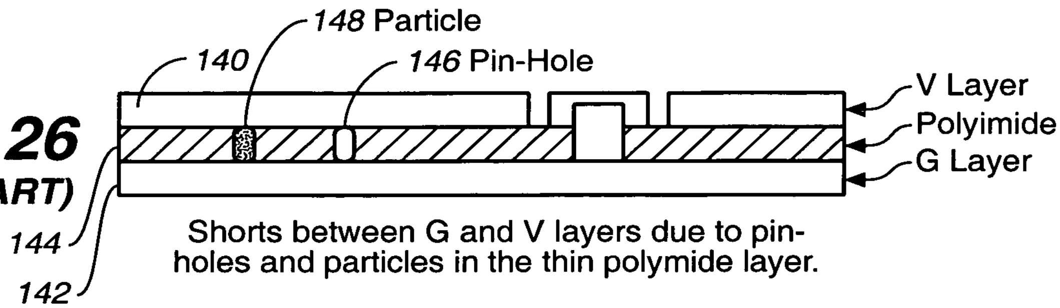
2. Illustration of close view of solder pedastal in contact with chip

FIG._25



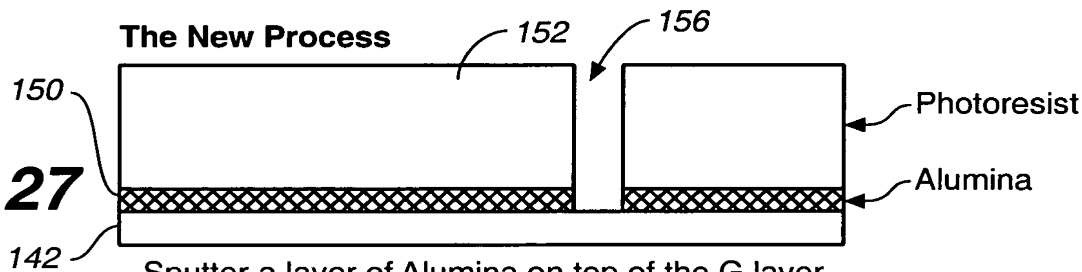
3. Illustration of top view of pedastal

FIG._26
(PRIOR ART)



Shorts between G and V layers due to pin-holes and particles in the thin polymide layer.

FIG._27



Sputter a layer of Alumina on top of the G layer.
Coat photoresist and pattern the photoresist.
Wet etch the Alumina using etchant such as EDTA.

FIG._28

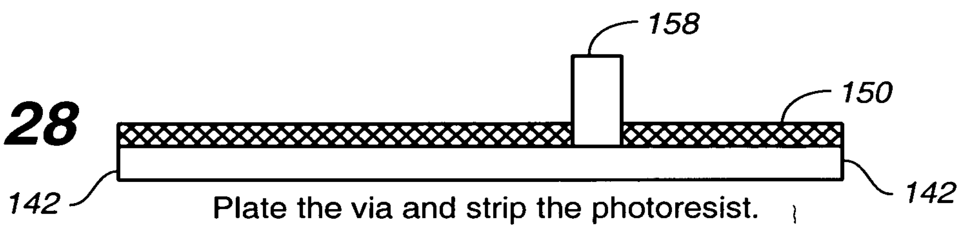
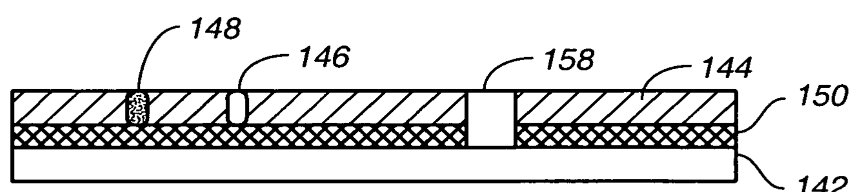


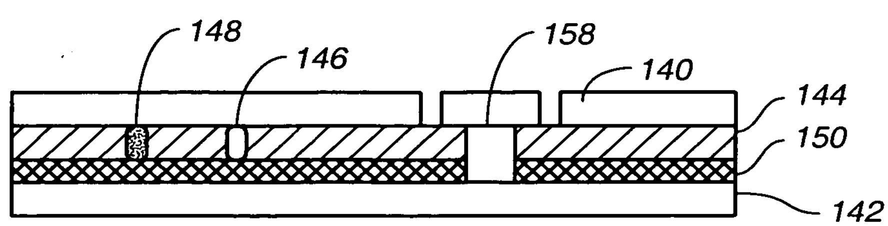
Plate the via and strip the photoresist.

FIG._29



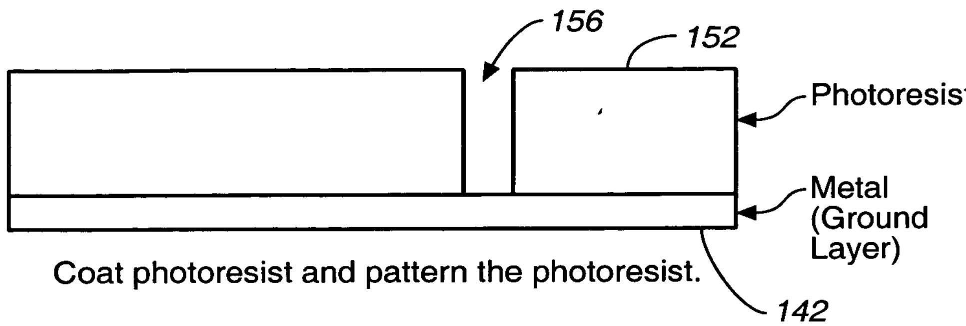
Coat polyimide, and then planarize and expose the vias.

FIG._30



Build V layer. Even if there are pin-holes and particles in the polyimide layer, no shorts occur between G and V layers.

FIG._31



Coat photoresist and pattern the photoresist.

FIG._32

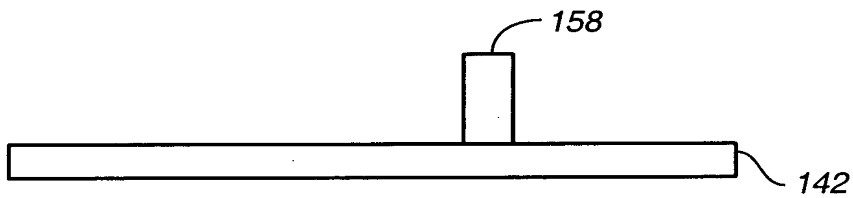
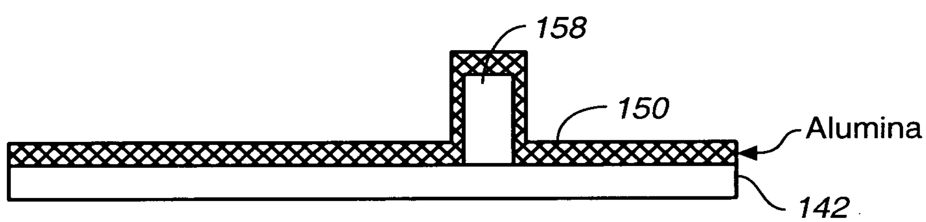


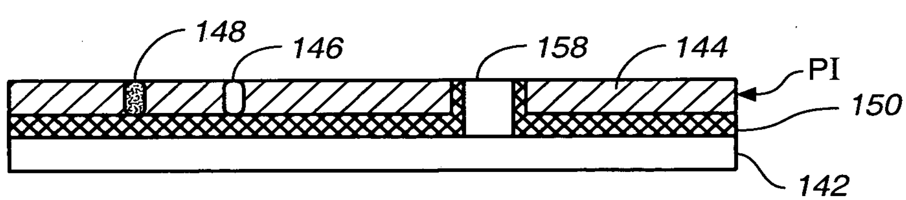
Plate vias, strip resist, and etch seed (if needed).

FIG._33



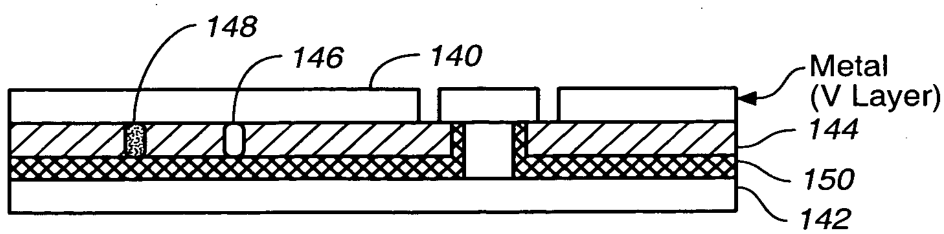
Deposit alumina (or other type of dielectric materials).
Deposition processes include CVD, PVD, or sol-gel process.

FIG._34



Coat PI layer and then planarize and expose the vias.

FIG._35



Build V layer. Even if there are pin-holes and particles in the polyimide layer, no shorts occur between G and V layers.

Coat a polyimide layer on top of a substrate. The substrate may be pre-treated for later film / substrate separation. Sputter Cr-Cu seed, and build up multi-layer circuits. The Cr-Cu seed layer is not removed until the film / substrate separation.

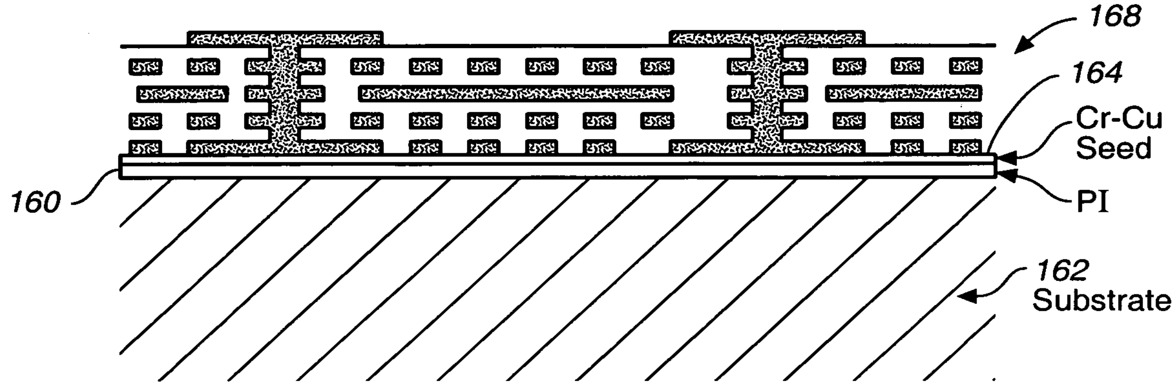


FIG._36

After film / substrate separation.

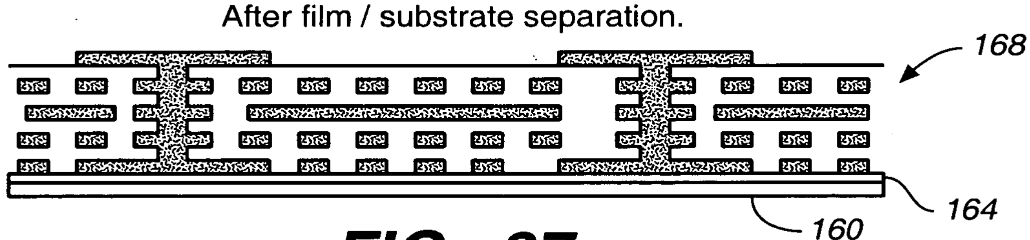


FIG._37

The polyimide layer is etched away using oxygen plasma. The Cr-Cu seed layer serves as the stop-layer for the plasma etching.

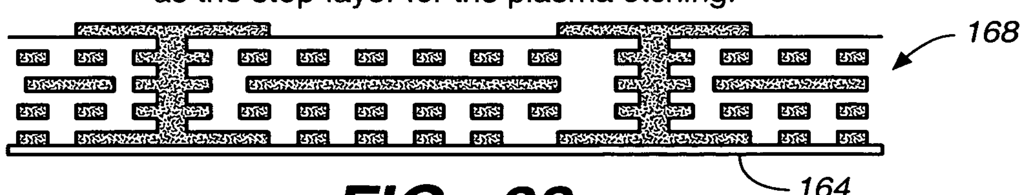


FIG._38

After wet etch of Cr-Cu seed.

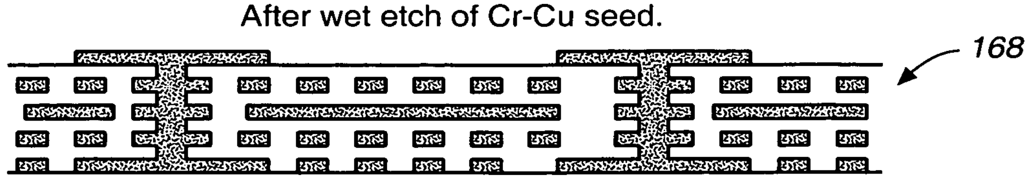


FIG._39

Coat a polyimide layer on top of a substrate and sputter Cr-Cu seed on top of the polyimide. The substrate may be pre-treatment for later film / substrate separation. The seed is etched away after completing the first metal pattern layer. Multi-layer circuits are then built.

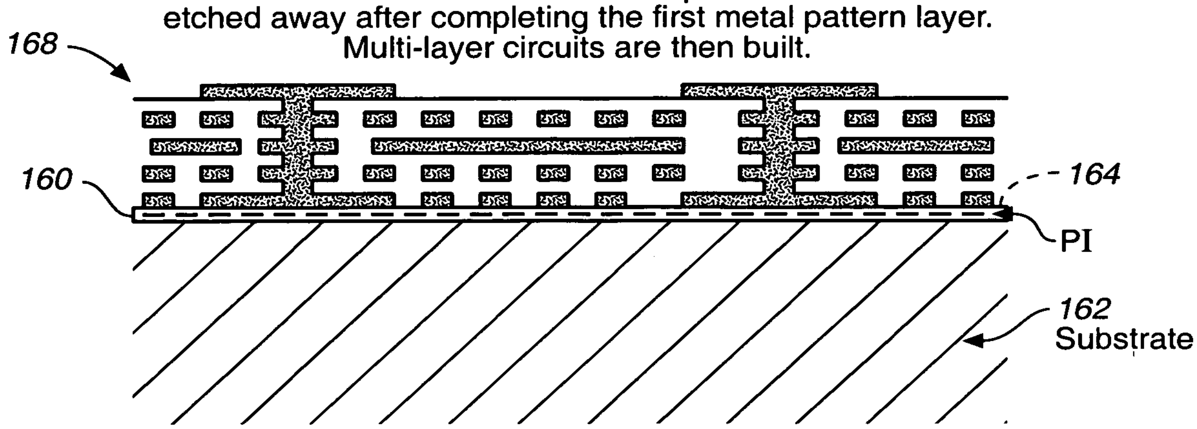


FIG._40

After film / substrate separation.

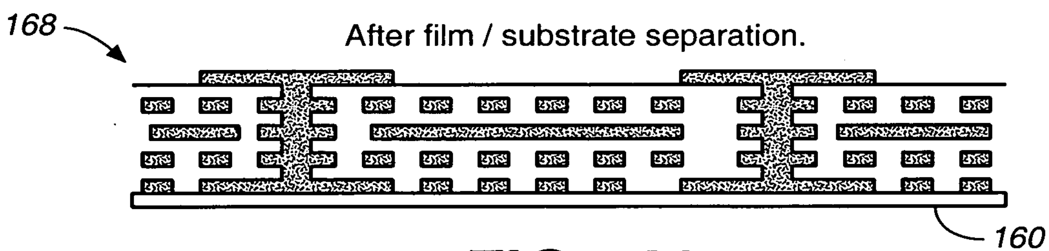


FIG._41

Using laser to open the pads.

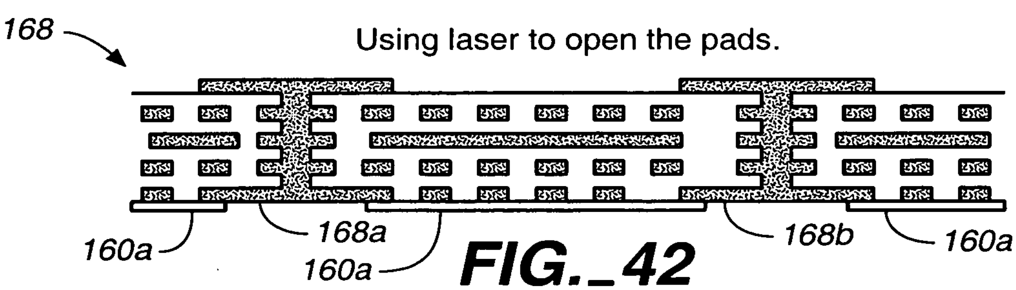


FIG._42

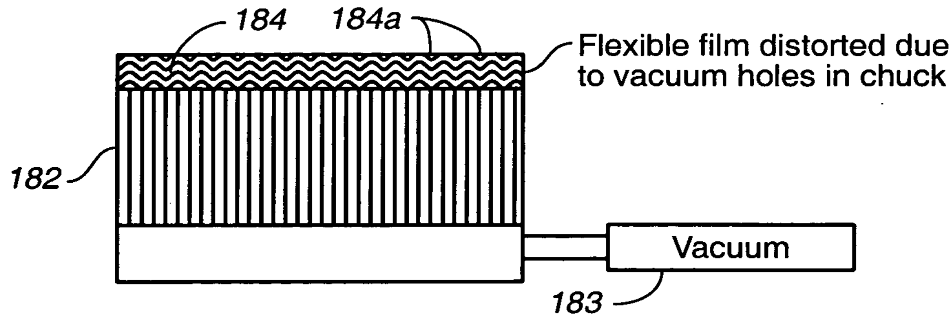


FIG._43

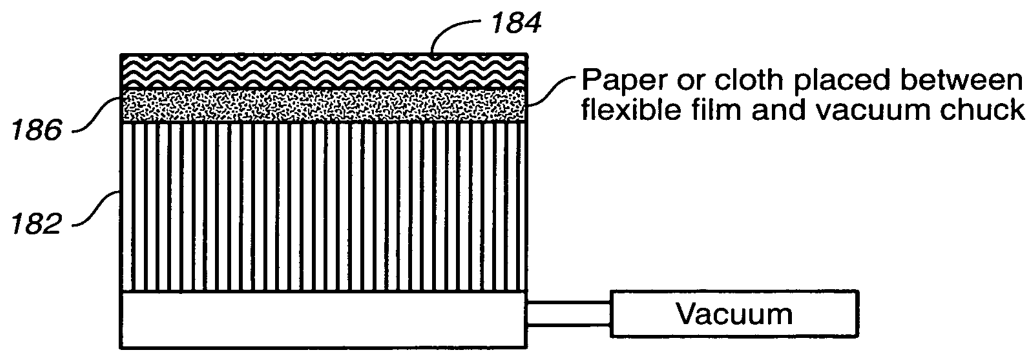
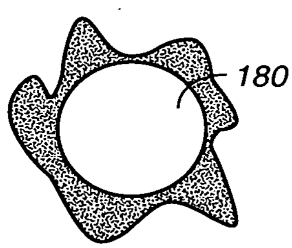
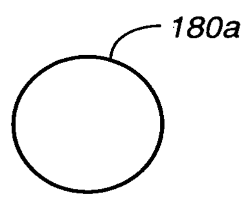


FIG._44



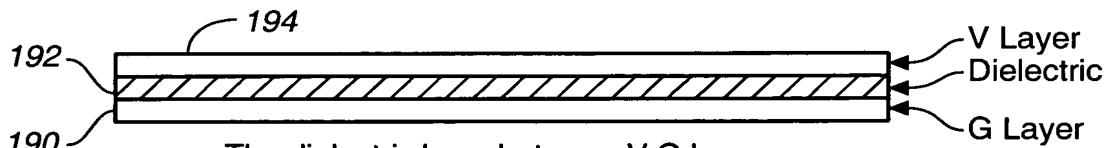
Bottom burn from laser ablation

FIG._45



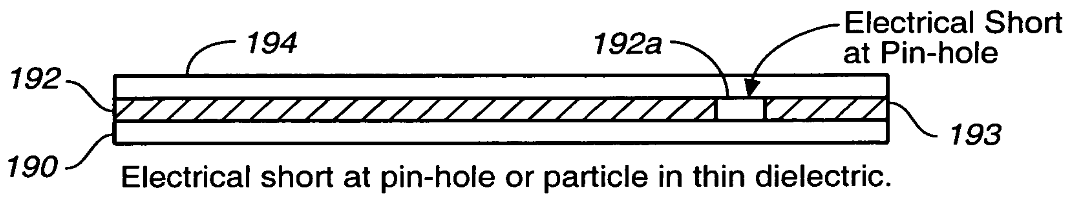
Burn reduced when paper or cloth is used

FIG._46



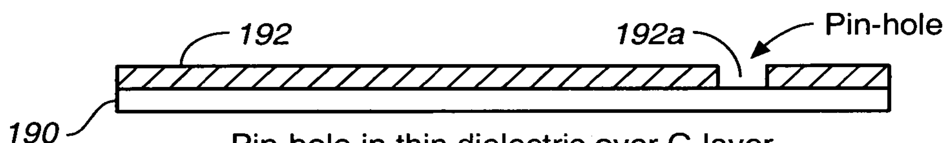
The dielectric layer between V-G layers.

FIG._47



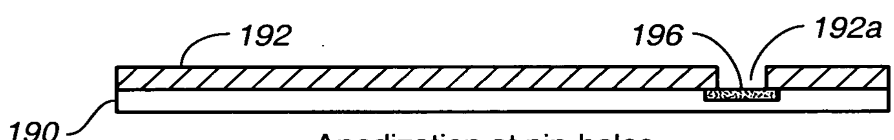
Electrical short at pin-hole or particle in thin dielectric.

FIG._48



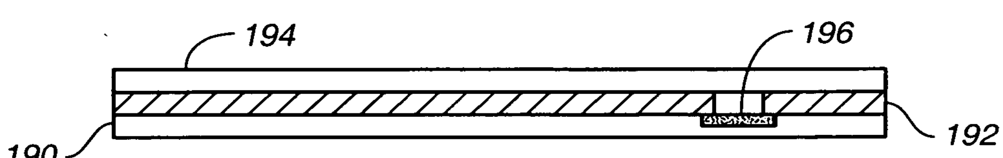
Pin-hole in thin dielectric over G layer.

FIG._49



Anodization at pin-holes.

FIG._50

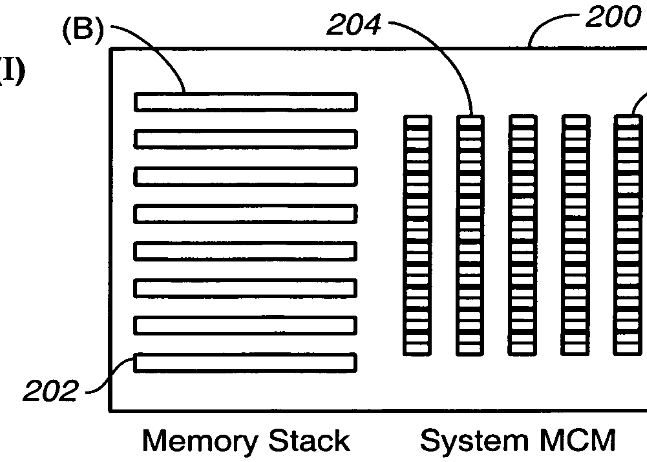


Oxide from anodization prevents electrical shorting at
pin-holes after deposition of top (V) metal layer.

FIG._51

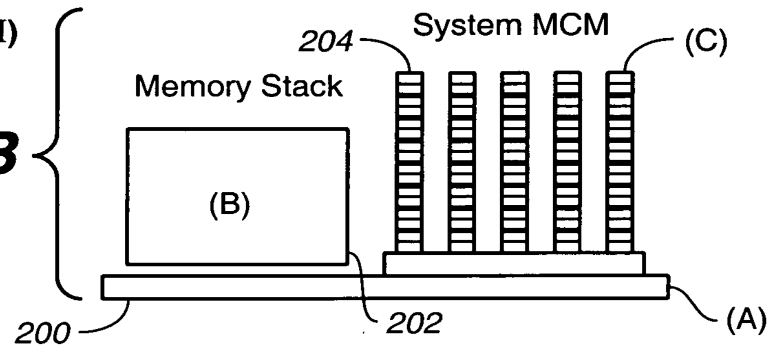
Case (I)

FIG._52A



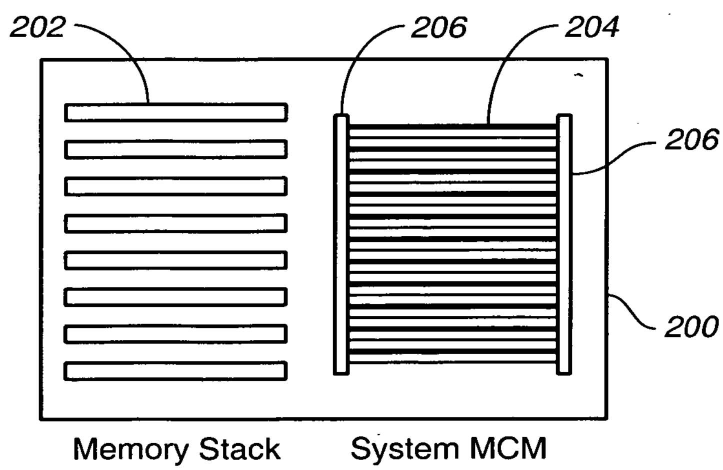
Case (I)

FIG._52B



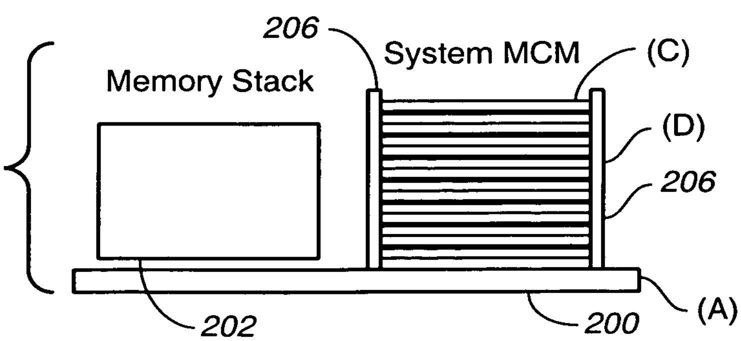
Case (II)

FIG._53A



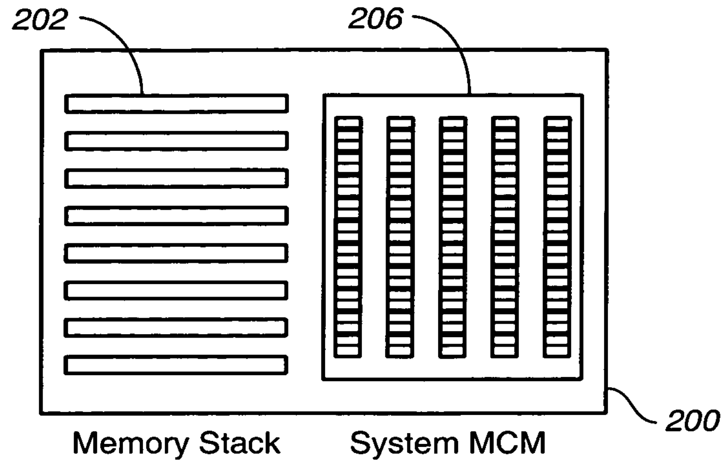
Case (II)

FIG._53B



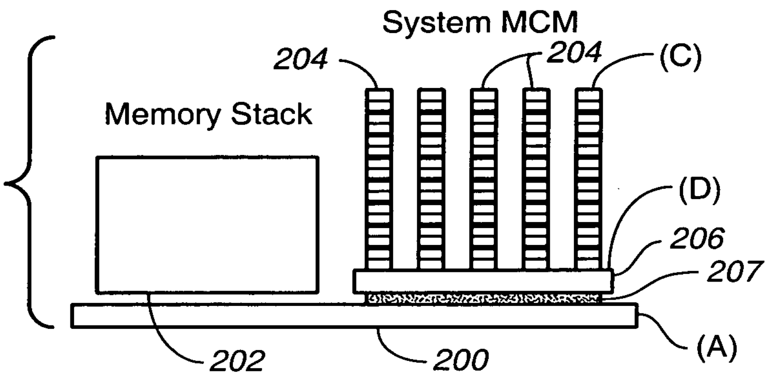
Case (III)

FIG._54A



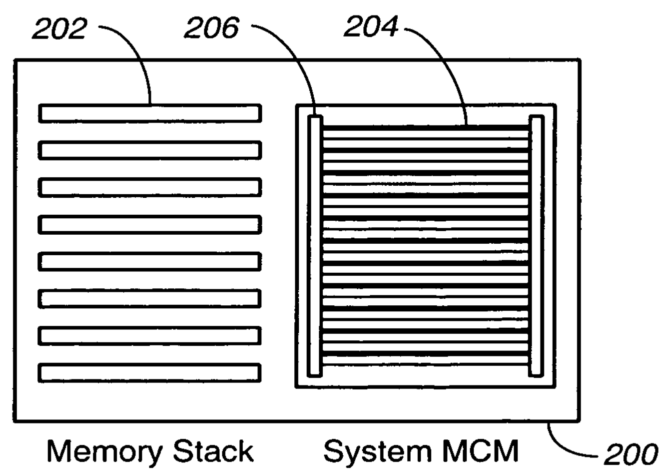
Case (III)

FIG._54B



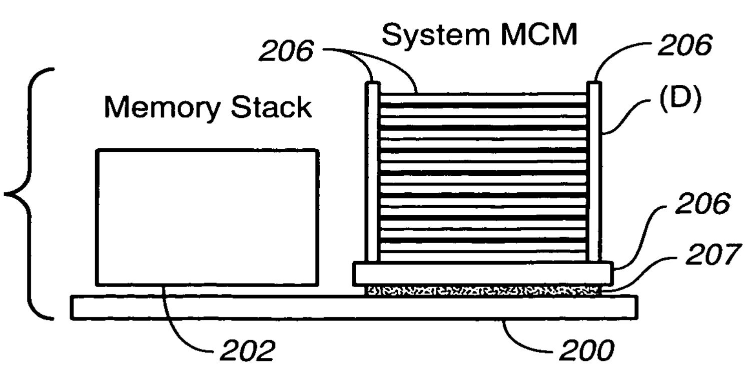
Case (IV)

FIG._55A



Case (IV)

FIG._55B



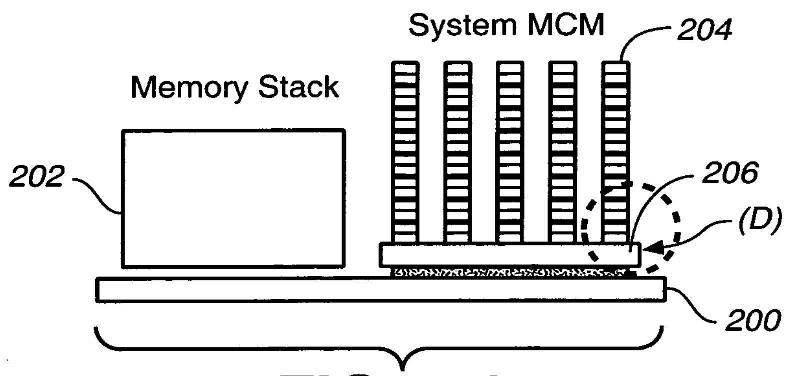

System MCM
204
Memory Stack
202
206
(D)
200

FIG._56

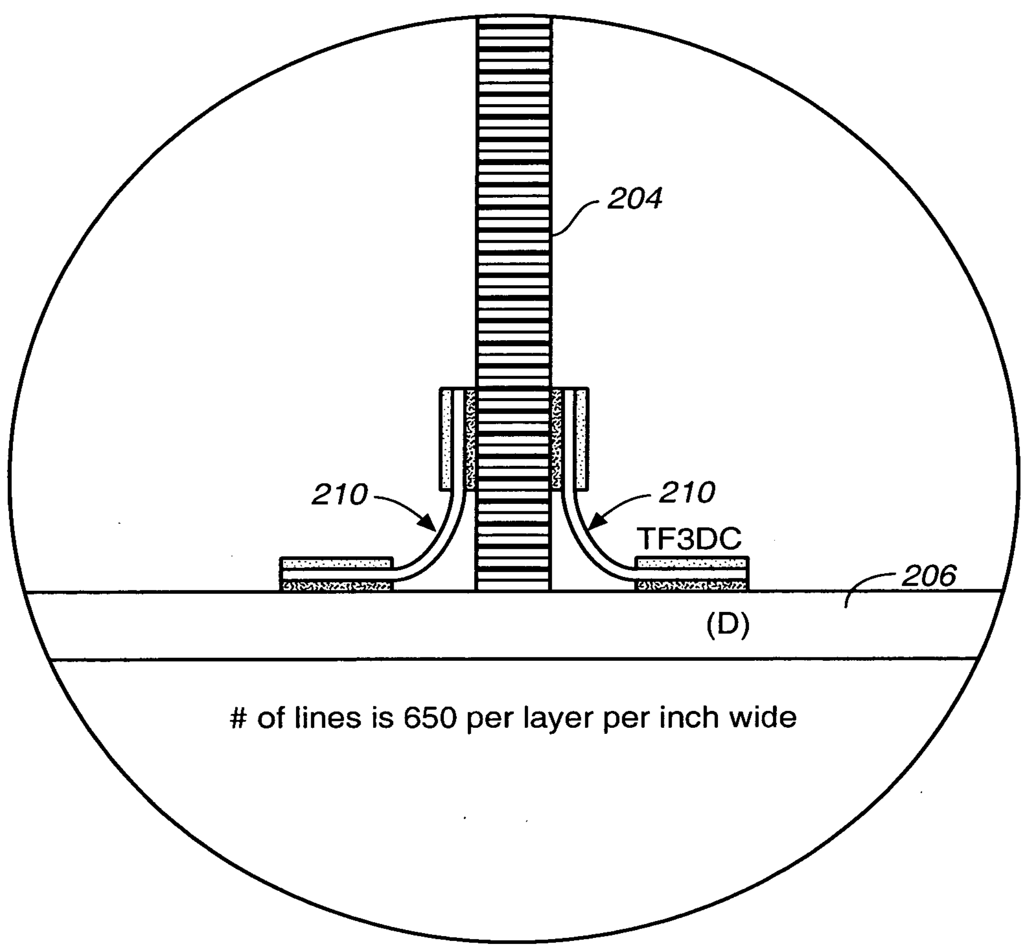

204
210
210
TF3DC
206
(D)
# of lines is 650 per layer per inch wide

FIG._57

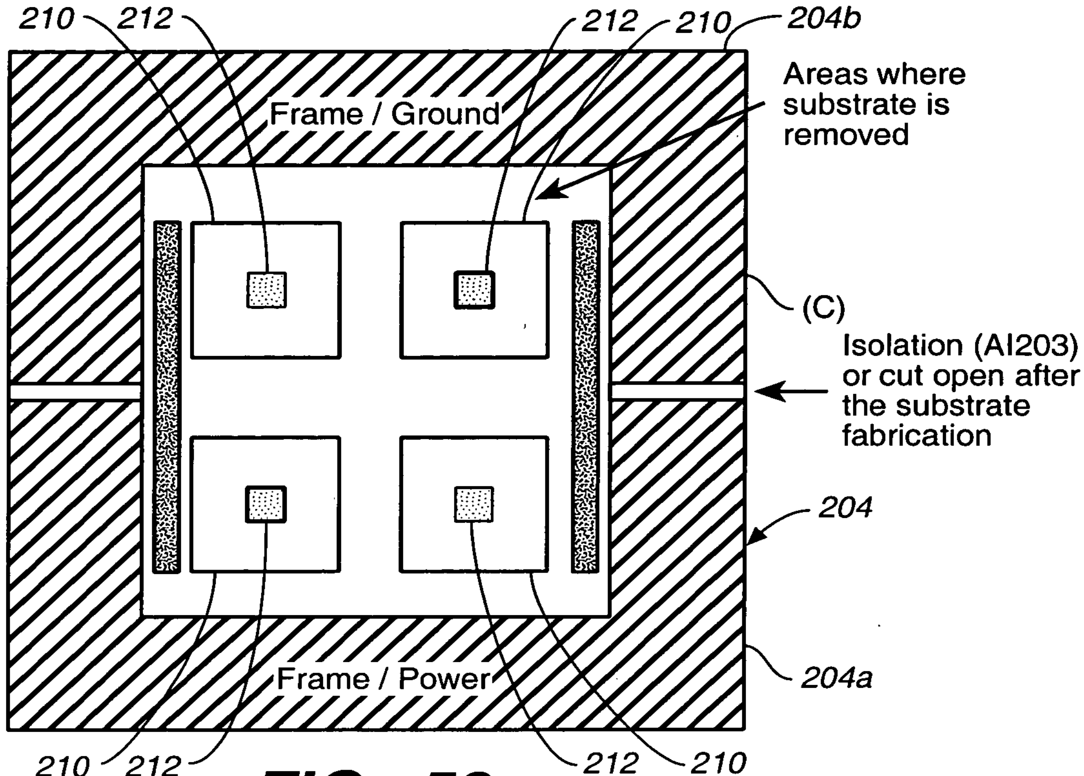


FIG._58

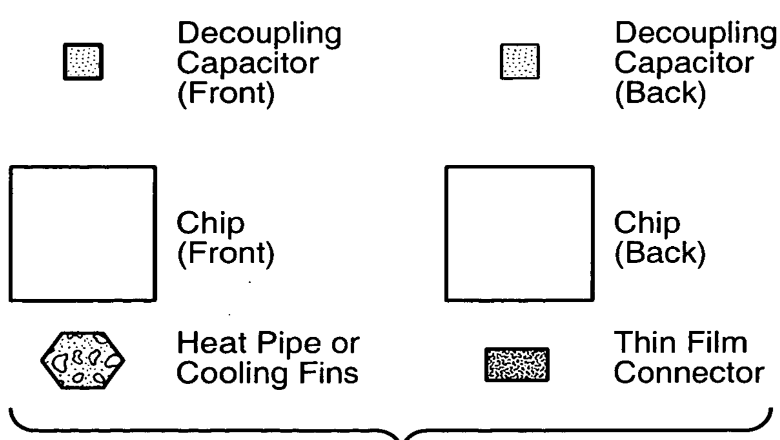


FIG._59

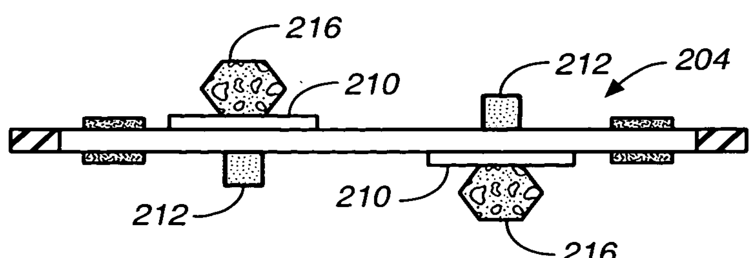


FIG._60

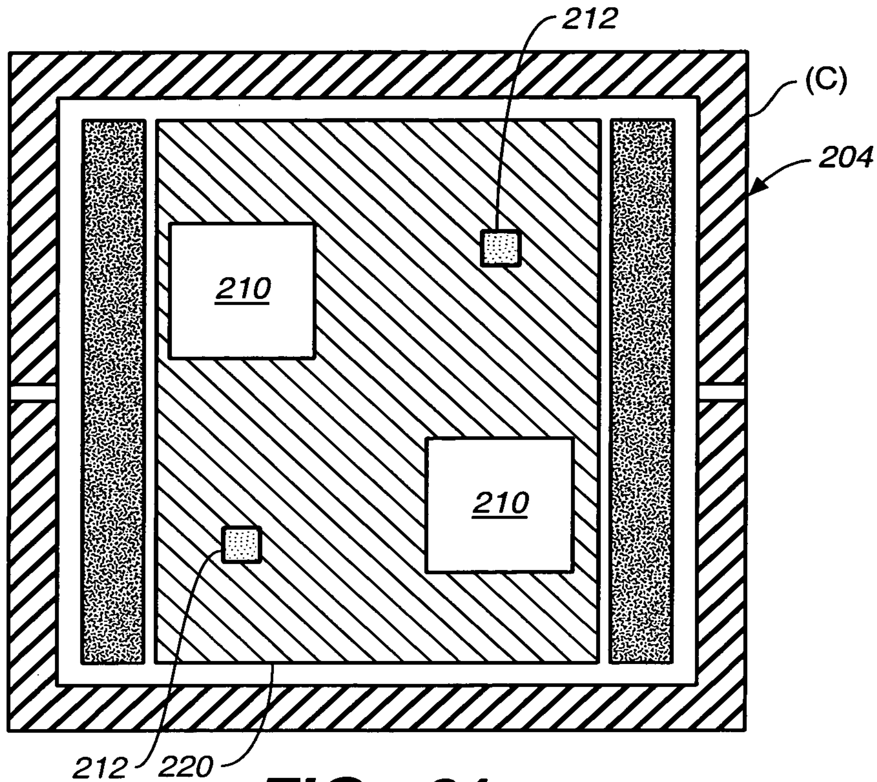


FIG._61

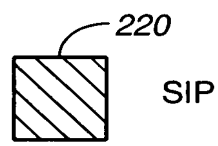


FIG._62

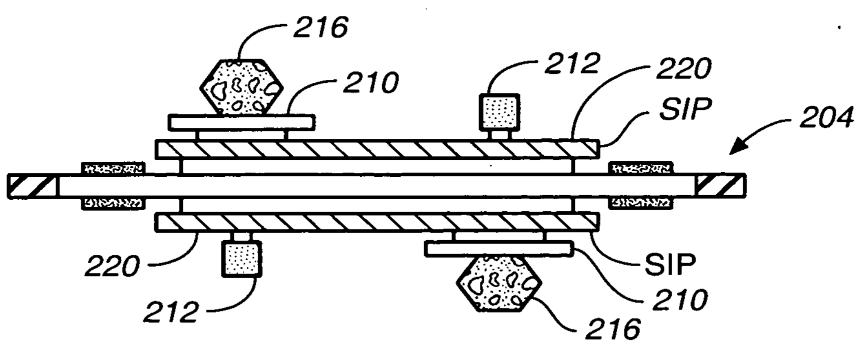


FIG._63

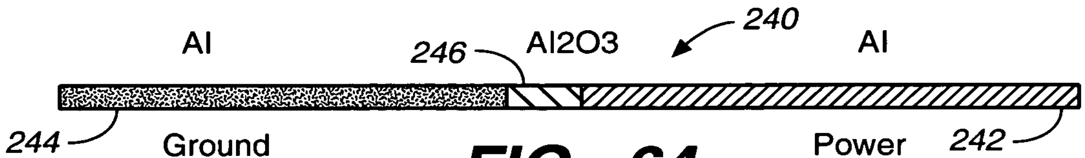


FIG._64

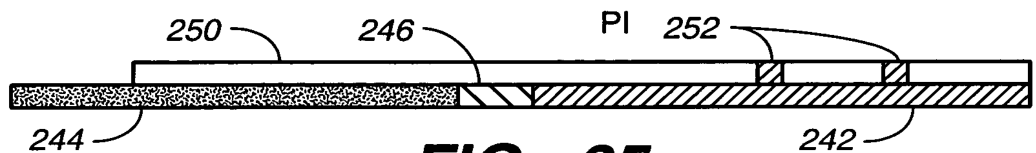


FIG._65

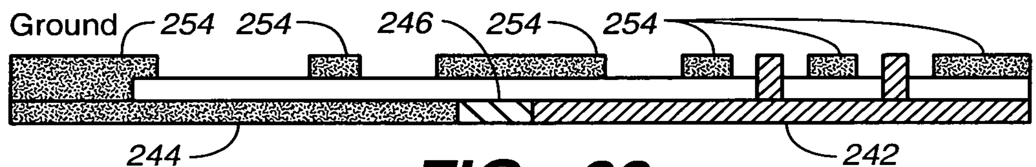


FIG._66

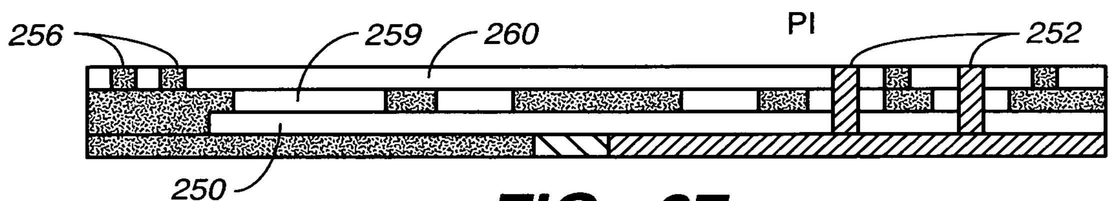


FIG._67

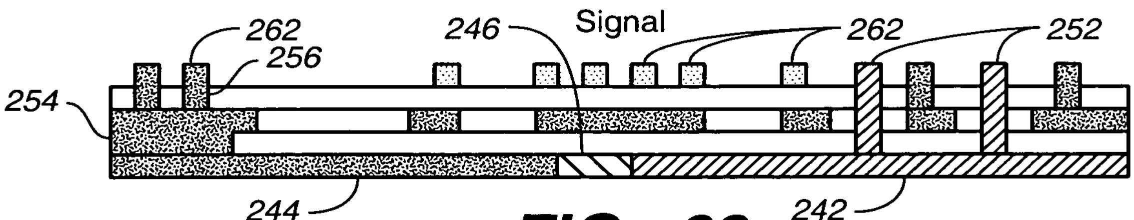


FIG._68

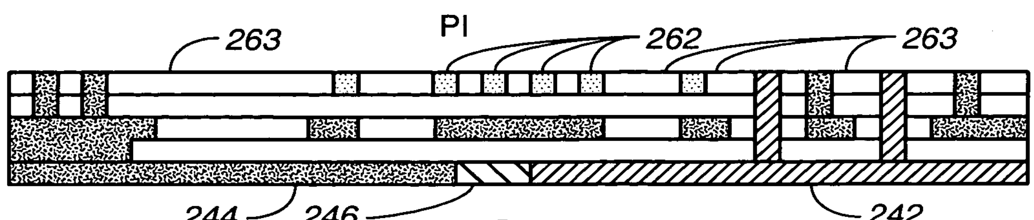


FIG._69

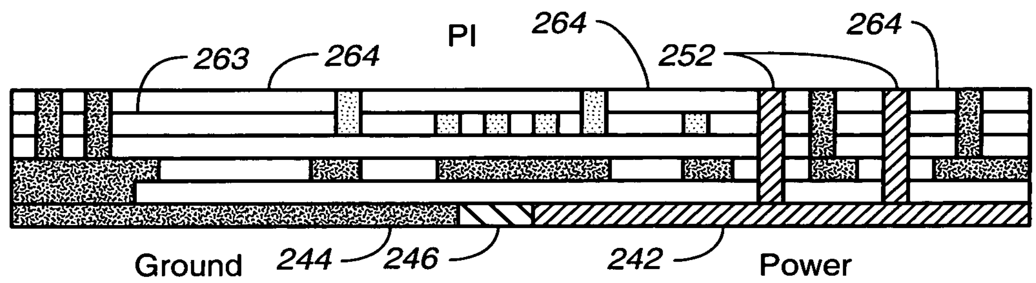


FIG._70

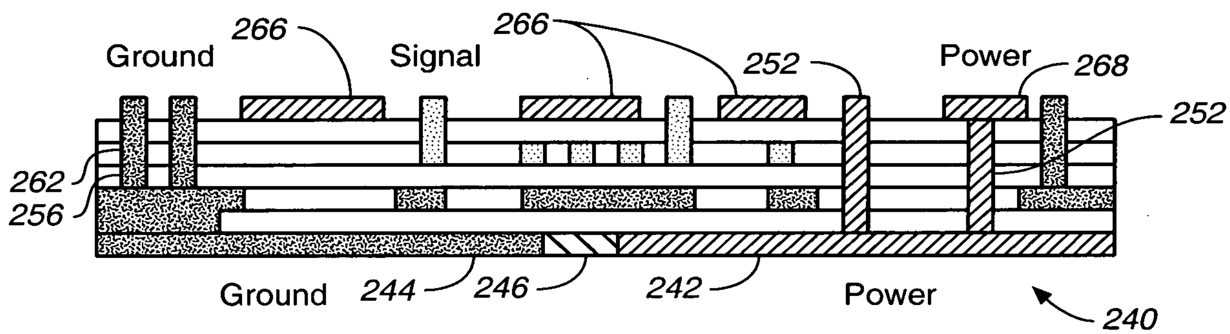


FIG._71

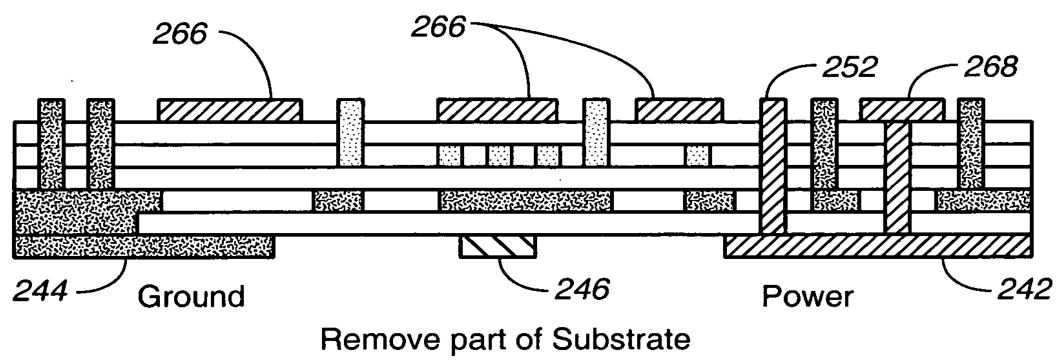


FIG._72

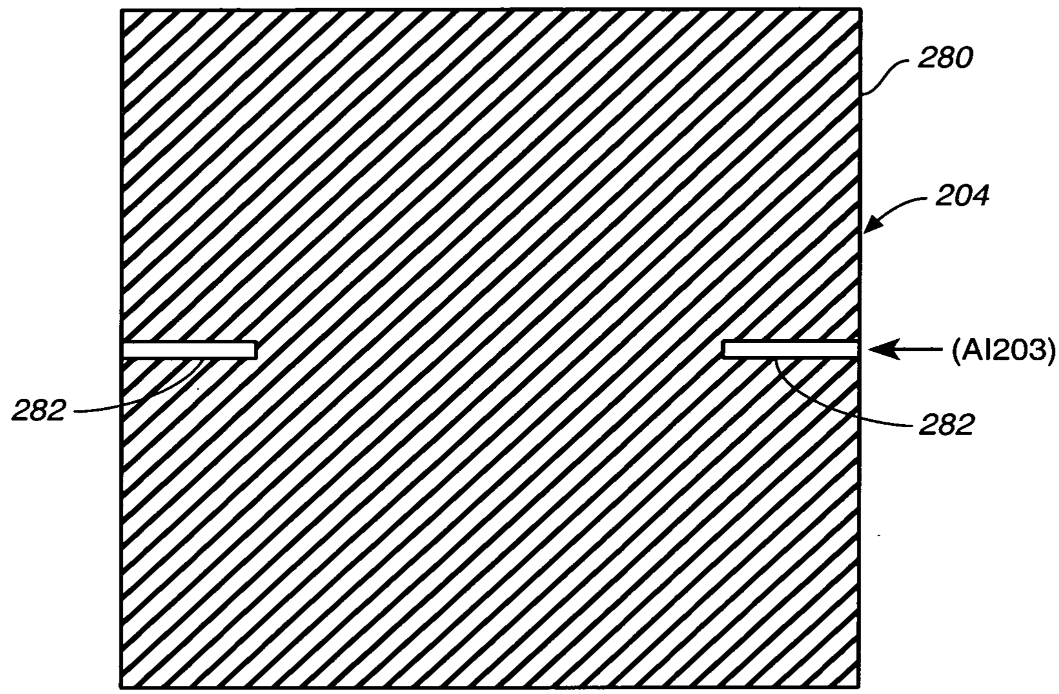


FIG._73

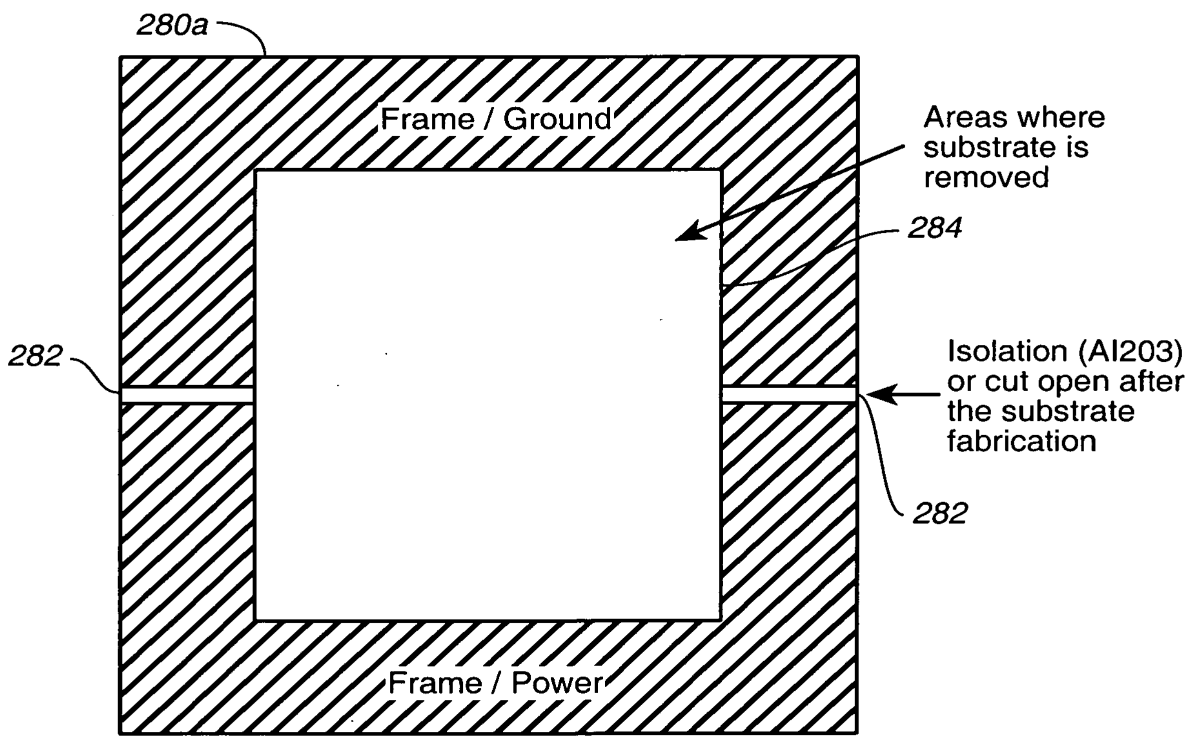


FIG._74

FIG._75

Traditional process for anisotropic conductive film (ACF) connection process for joining two substrate.

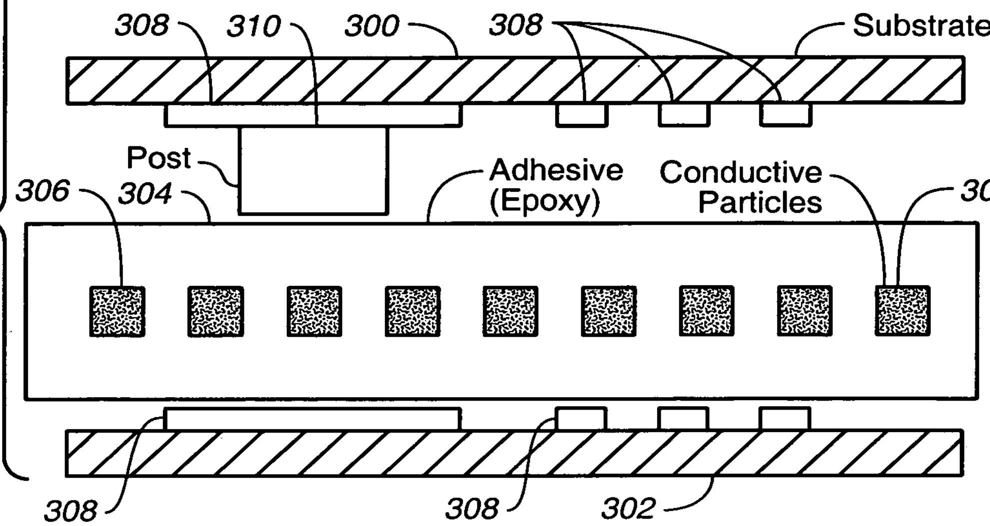


FIG._76

Traditional process for anisotropic conductive film (ACF) connection process for joining two substrate.

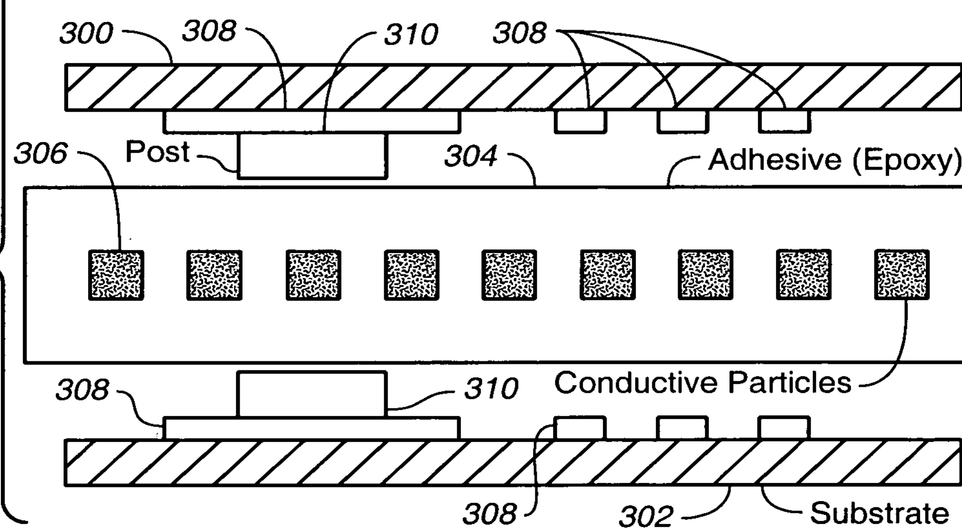


FIG._77

AFC connection after lamination under high pressure and high temperature in traditional ACF process.

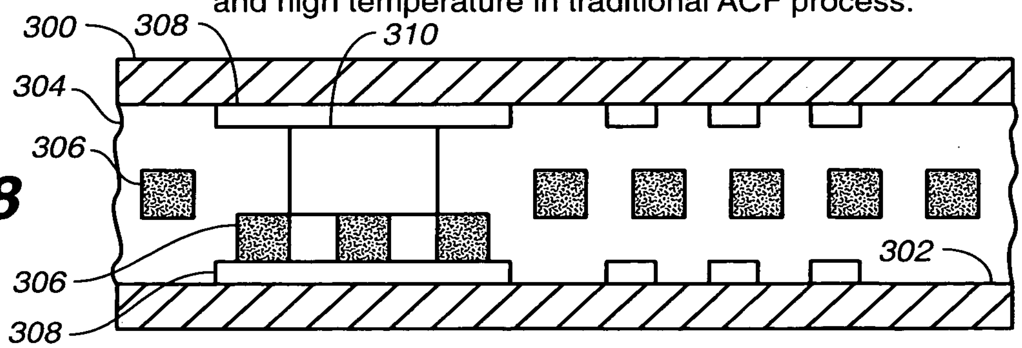


FIG._78

AFC connection after lamination under high pressure and high temperature in traditional ACF process.

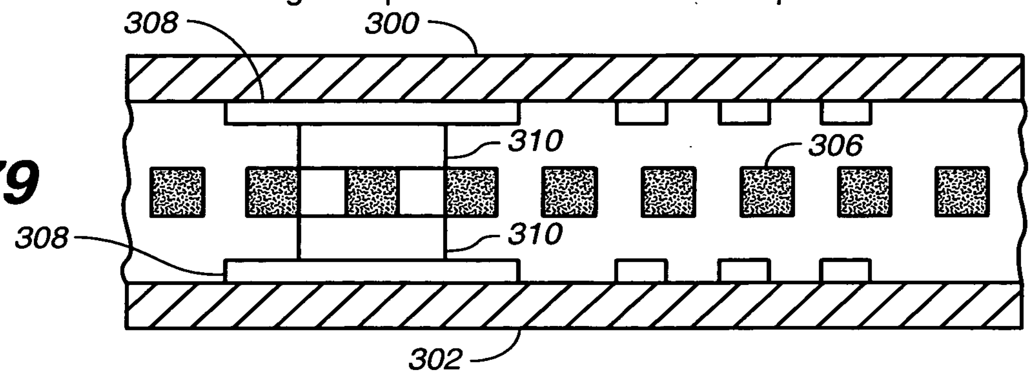


FIG._79

Low resistance ACF joints by depositing a thin layer of low melting point metal that will form intermetallic compound / alloy between post material and conductive particles in ACF.

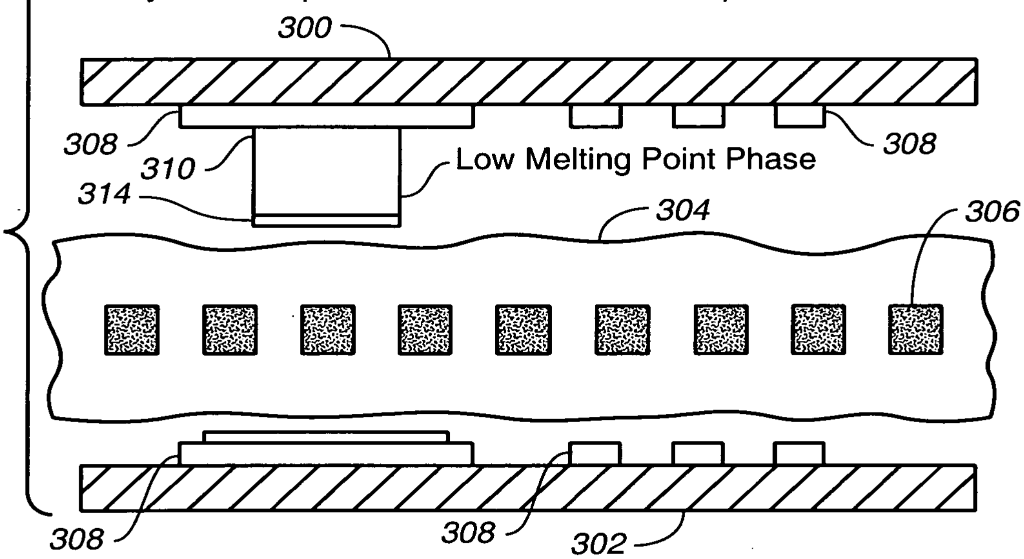


FIG._80

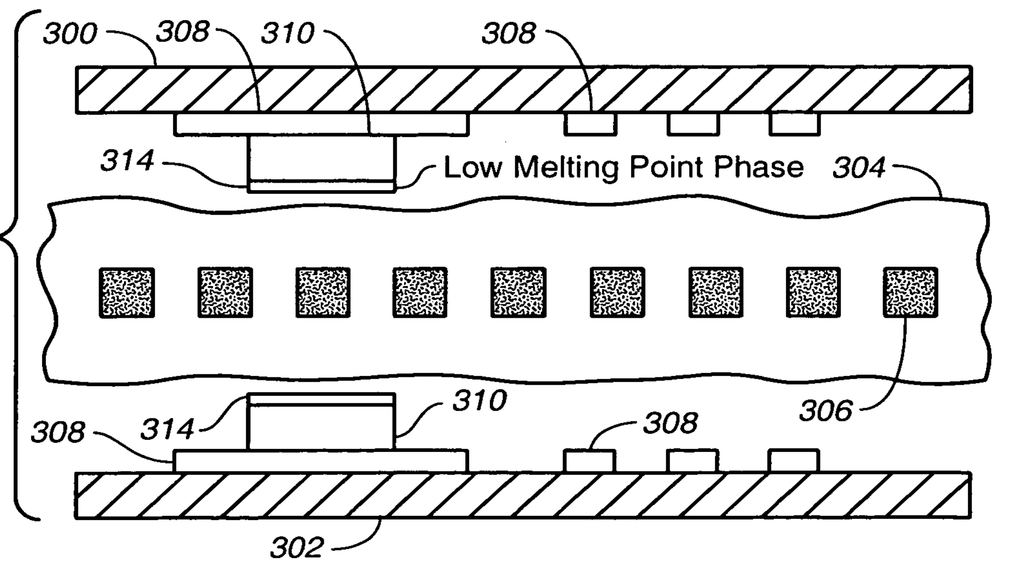


FIG._81

After joining process (high pressure and high temperature), intermetallic / alloy formed at the interface of post and conductive particles. The intermetallic / alloy will decrease the contact resistance from traditional ACF process and provide a stronger mechanical bond.

FIG._82

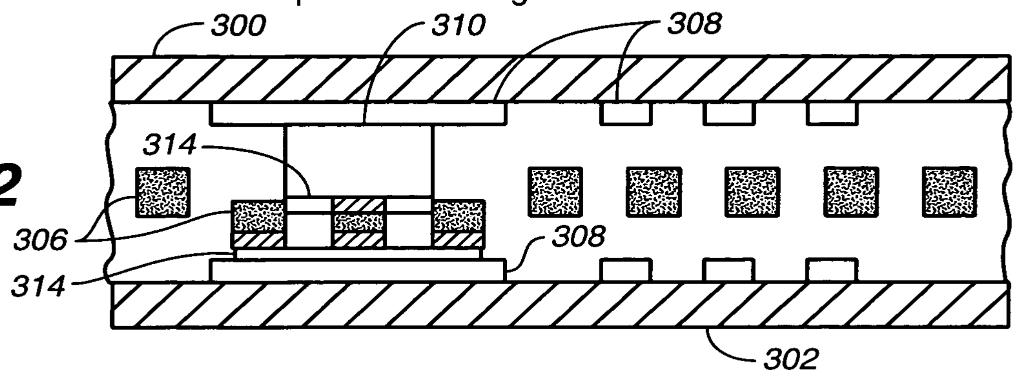
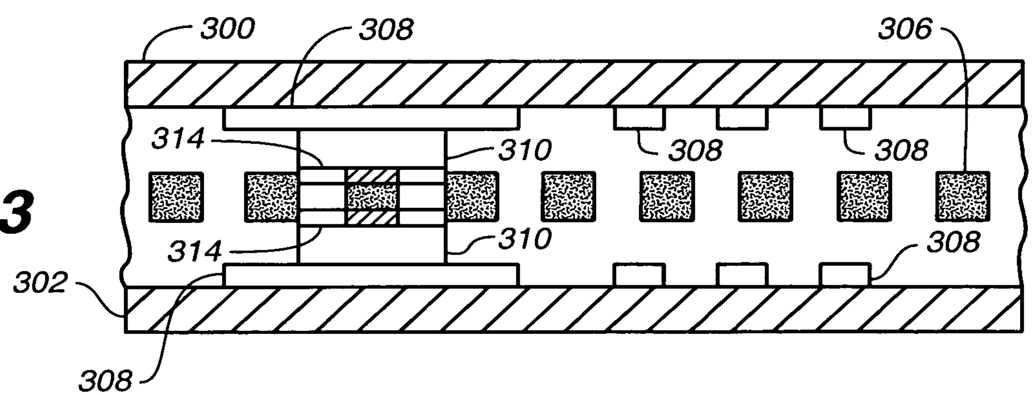


FIG._83



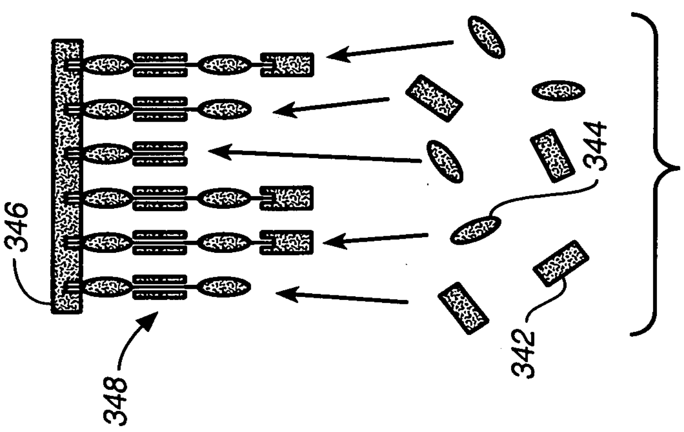


FIG._84B

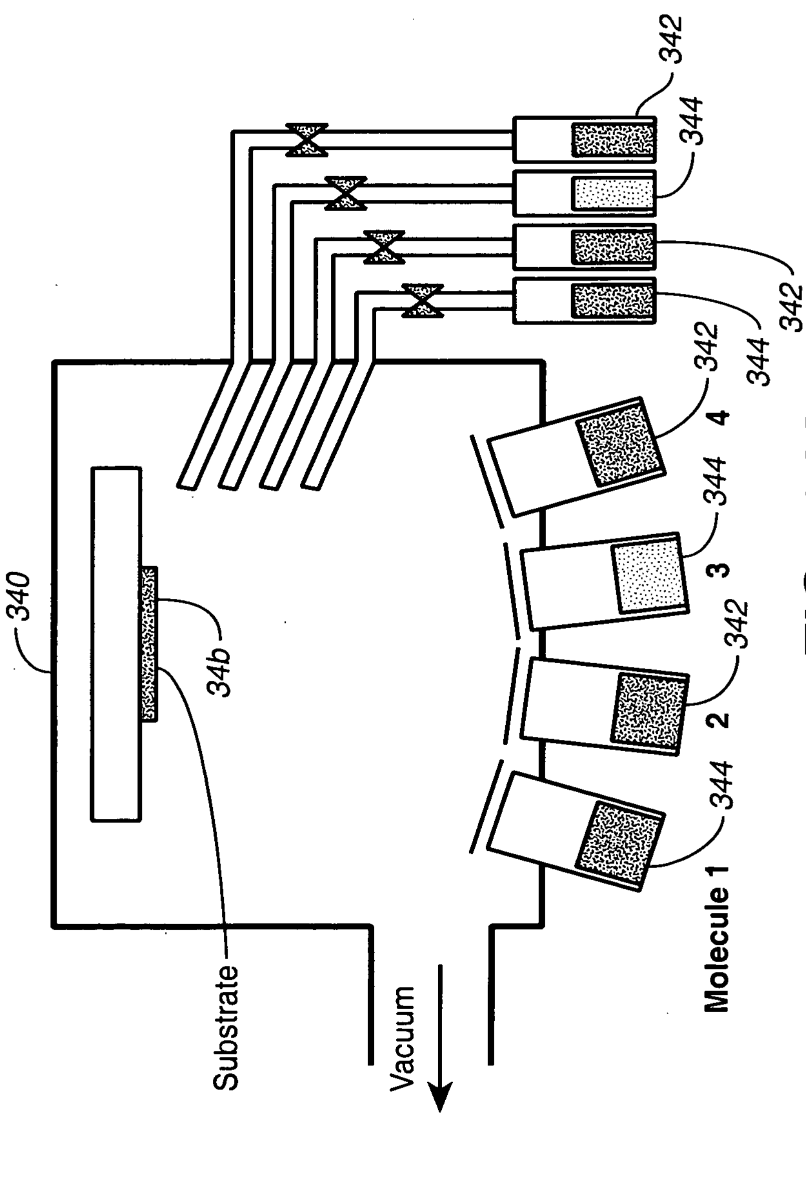


FIG._84A

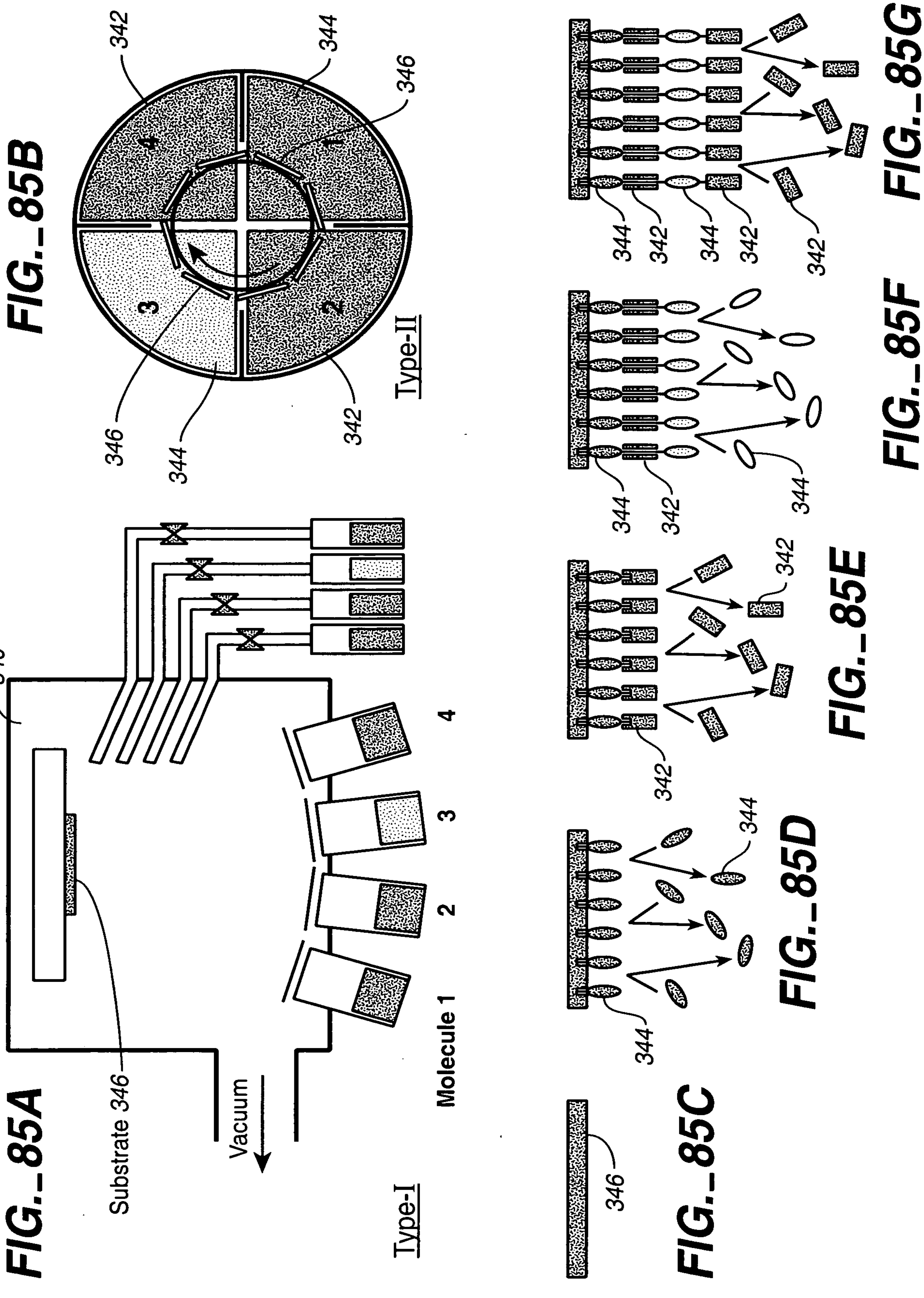


FIG._85A

FIG._85B

FIG._85C

FIG._85D

FIG._85E

FIG._85F

FIG._85G

FUJITSU Computer Packaging Technologies, Inc. FCPT

Vapor Phase Deposition Vs. Spin Coating

	Spin Coating	Vapor Phase Deposition	
		CVD	MLD
-Coverage Controllability	Low	High	High
-Thickness Accuracy / Uniformity	Low	Medium	High
-Deposition Rate	High	Medium	Low
-Molecular-level Controllability	Low	Medium	High
-Selective / Deposition	No	Yes	Yes
-Selective Molecular Alignment	No	Yes	Yes

(High & Yes are preferable)

-Conformable coverage and Thickness accuracy / uniformity
-CVD / MLD are superior to Spin Coating

-Low ε insulator with strong adhesion
-MLD may provide high adhesion with the Molecular-Level Controllability

-Options
-CVD / MLD can do #Selective Deposition (hydrophilic / hydrophobic surface)
#Selective Molecular Alignment (surface treatment)
may provide further ε reduction, process simplification, and low Cu-diffusion

$\underbrace{\hspace{20em}}$

FIG._85H

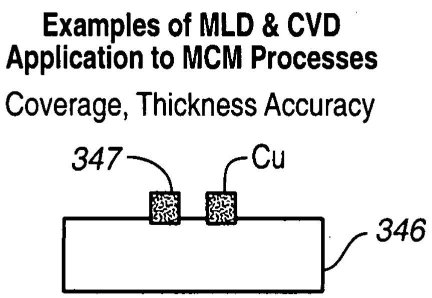


FIG._86A

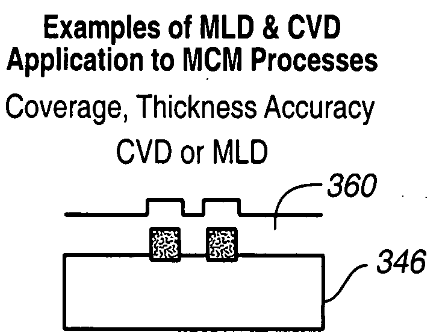


FIG._86B

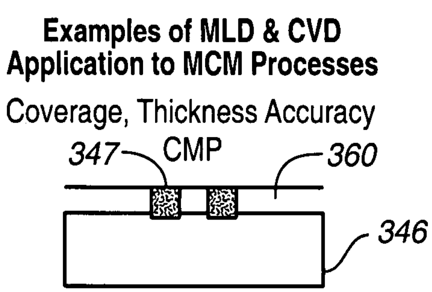


FIG._86C

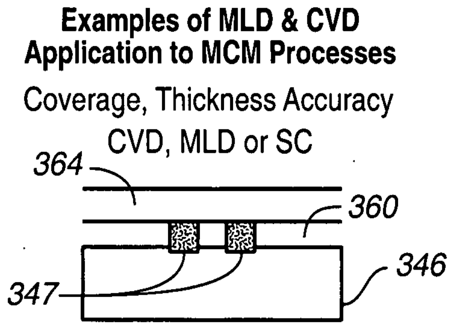


FIG._86D

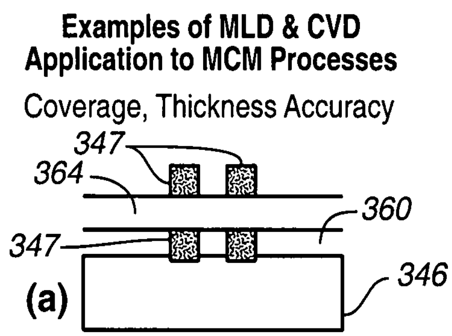


FIG._86E

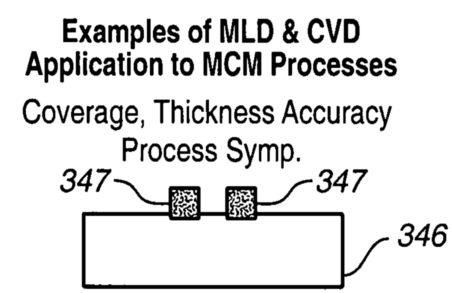


FIG._86F

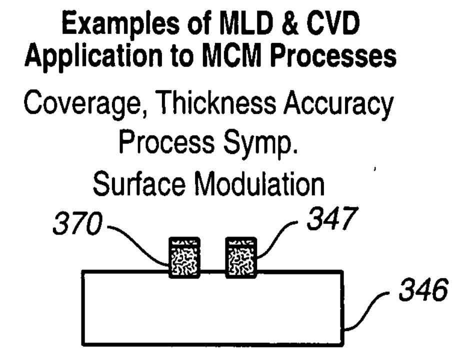


FIG._86G

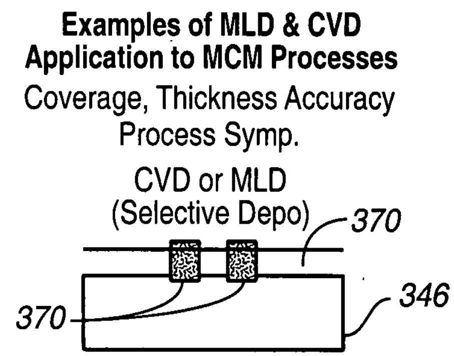


FIG._86H

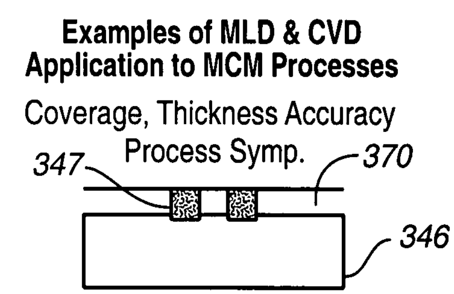


FIG._86I

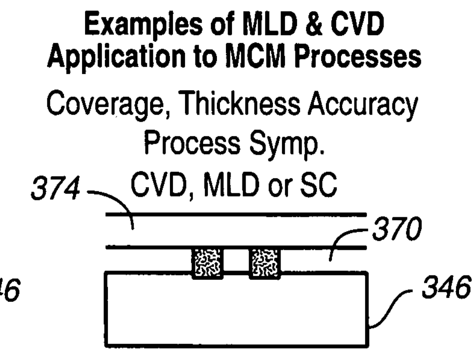


FIG._86J

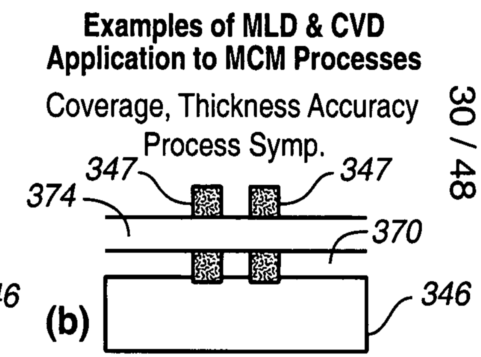


FIG._86K

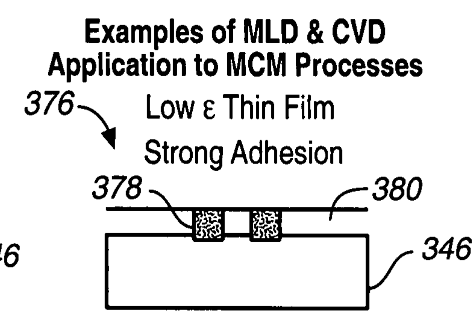


FIG._86L

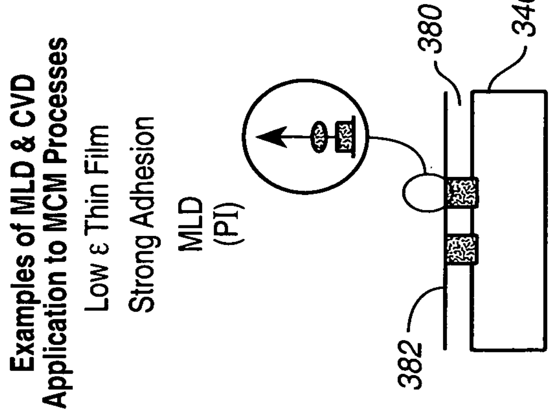


FIG._86M

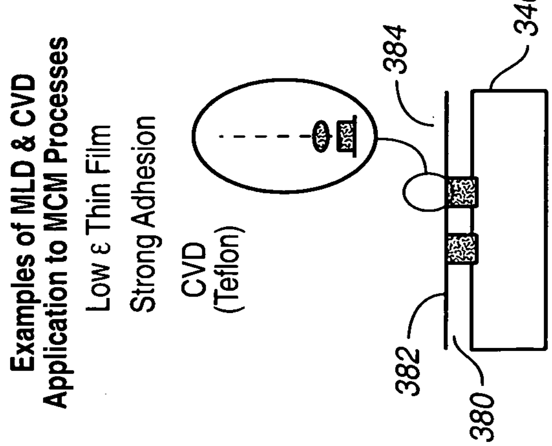


FIG._86N

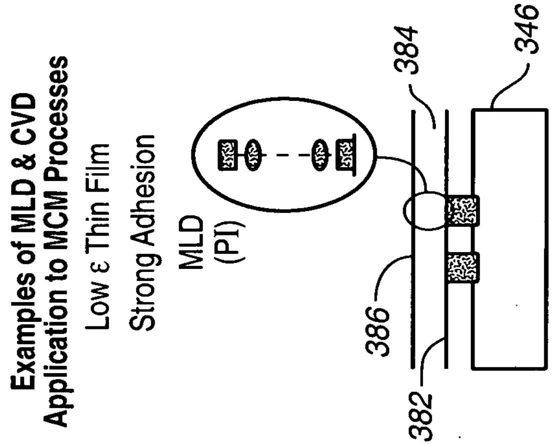


FIG._86O

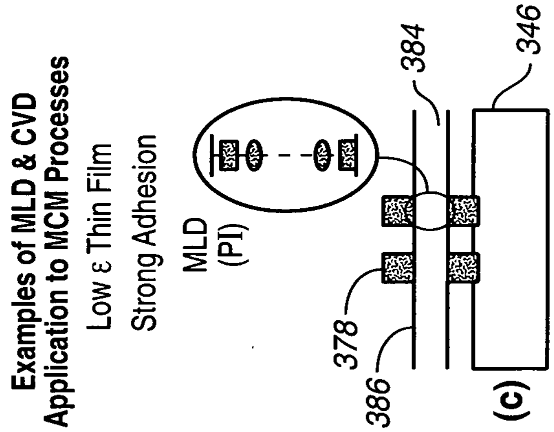


FIG._86P

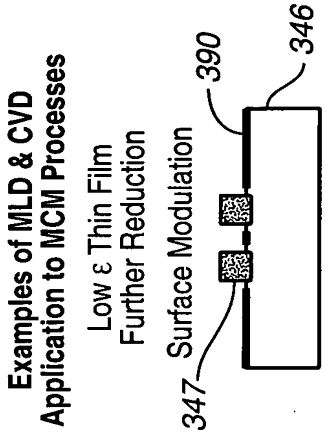


FIG._86Q

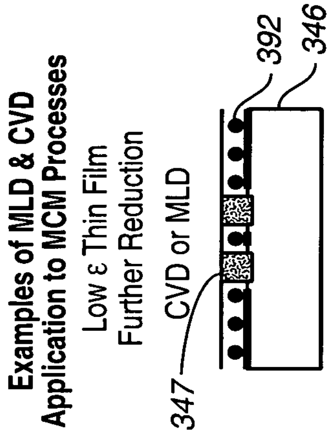


FIG._86R

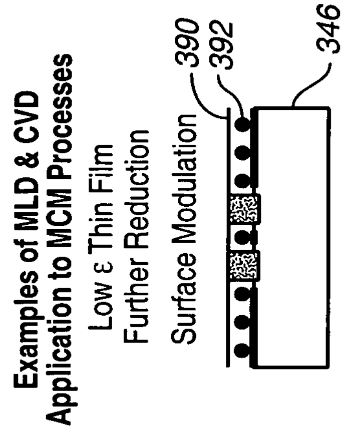


FIG._86S

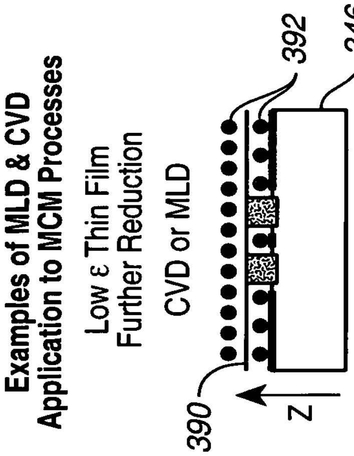


FIG._86T

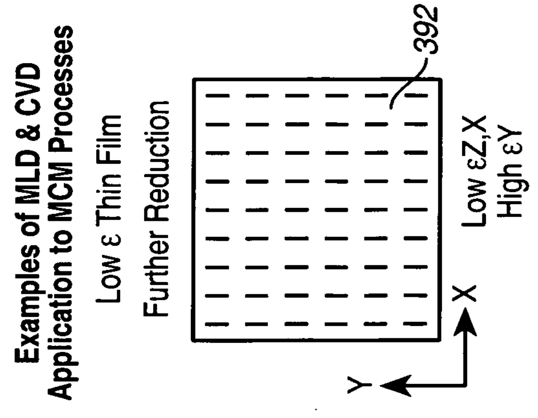


FIG._86U

Examples of MLD & CVD Application to MCM Processes

Low ε Thin Film

Further Reduction

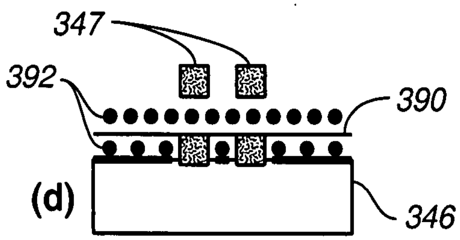


FIG._86V

Examples of MLD & CVD Application to MCM Processes

Low Water Absorption
Low Cu-Diffusion
Appropriate CTE
ε-modulation

CVD or MLD

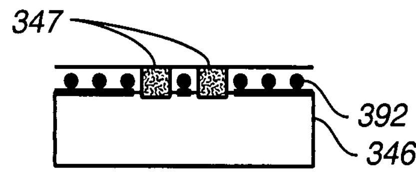


FIG._86X

Examples of MLD & CVD Application to MCM Processes

Low Water Absorption
Low Cu-Diffusion
Appropriate CTE
ε-modulation

CVD or MLD

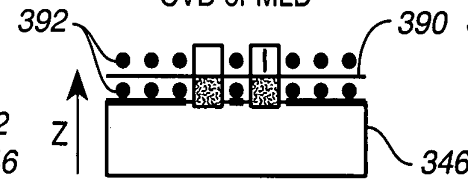


FIG._86Z

Examples of MLD & CVD Application to MCM Processes

Low Water Absorption
Low Cu-Diffusion
Appropriate CTE
ε-modulation

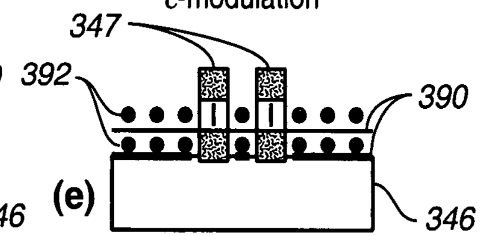


FIG._86BB

Examples of MLD & CVD Application to MCM Processes

Low Water Absorption
Low Cu-Diffusion
Appropriate CTE
ε-modulation

Surface Modulation

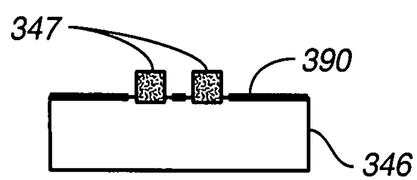


FIG._86W

Examples of MLD & CVD Application to MCM Processes

Low Water Absorption
Low Cu-Diffusion
Appropriate CTE
ε-modulation

Surface Modulation

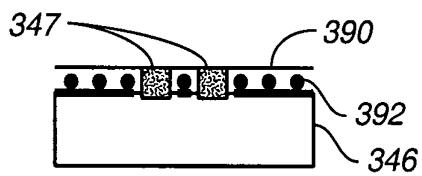


FIG._86Y

Examples of MLD & CVD Application to MCM Processes

Low Water Absorption
Low Cu-Diffusion
Appropriate CTE
ε-modulation

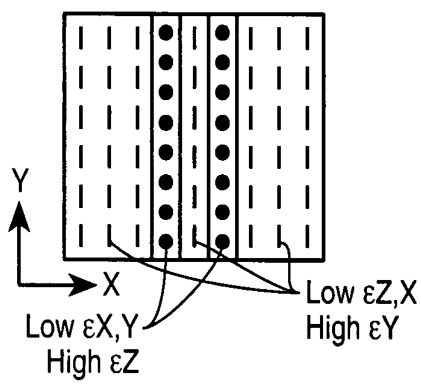
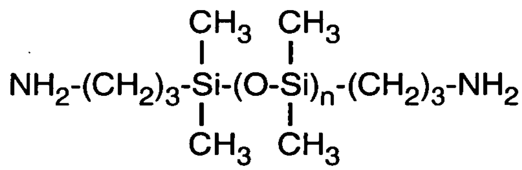


FIG._86AA

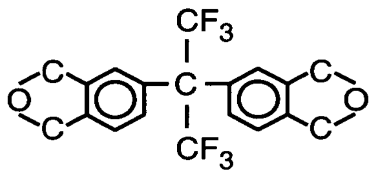
PMDA

ODA

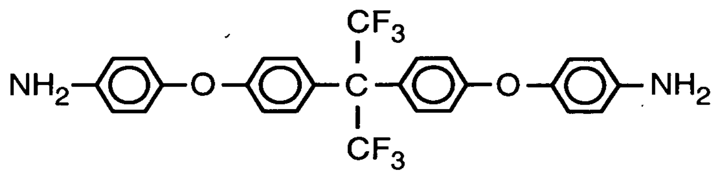
naphthalene dianhydride (ND)



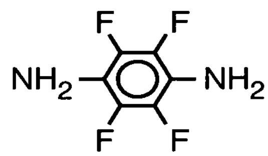
SiDA



6FDA



Bis-OAF



VT4-DA

alkylamine-coated Si | ND → Bis-OAF → ND → Bis-OAF → ••• → ND → SiDA

Si | SiDA → 6FDA → Bis-OAF + 6FDA → SiDA

Si | SiDA → ODA → 6FDA → VT4-DA → 6FDA → ••• → ODA → SiDA

FIG._86CC

Process Flow of the Resist-free Electroplated Solder Reflow Process

1. Masking

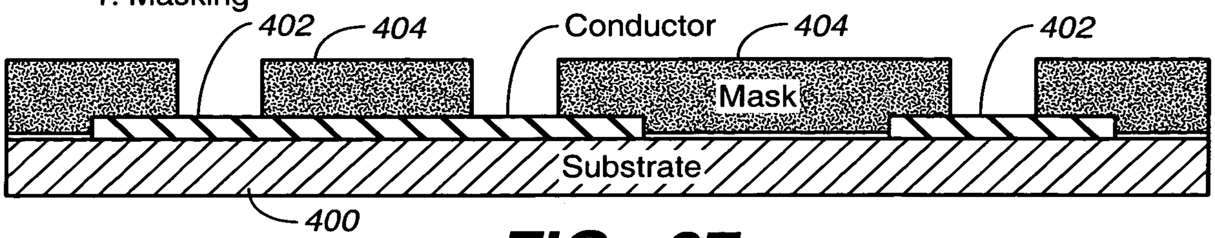


FIG._87

Process Flow of the Resist-free Electroplated Solder Reflow Process

2. Electroplating Solder

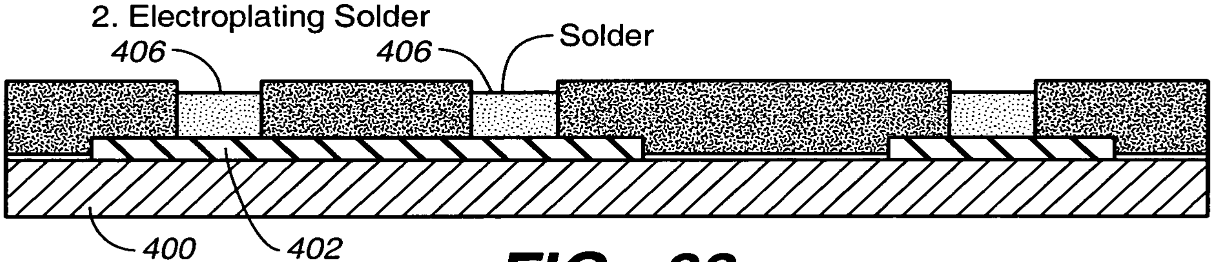


FIG._88

Process Flow of the Resist-free Electroplated Solder Reflow Process

3. Mask Strip

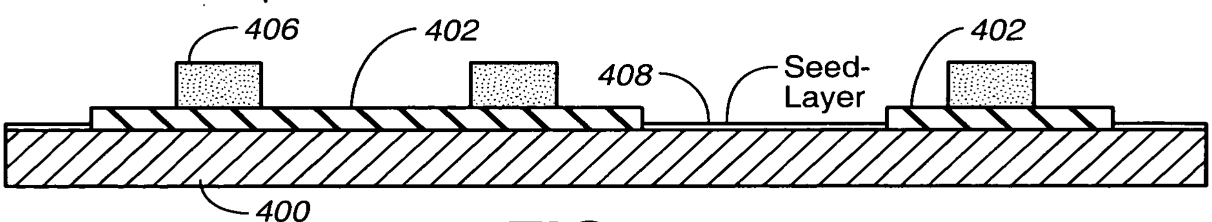


FIG._89

Process Flow of the Resist-free Electroplated Solder Reflow Process

4. Seed Etch

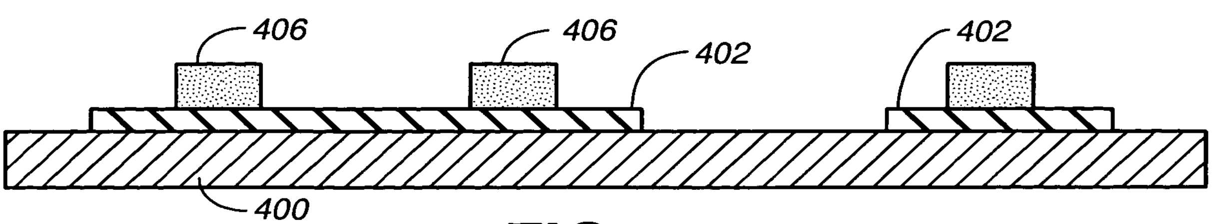


FIG._90

Process Flow of the Resist-free Electroplated Solder Reflow Process

5. Fluxing

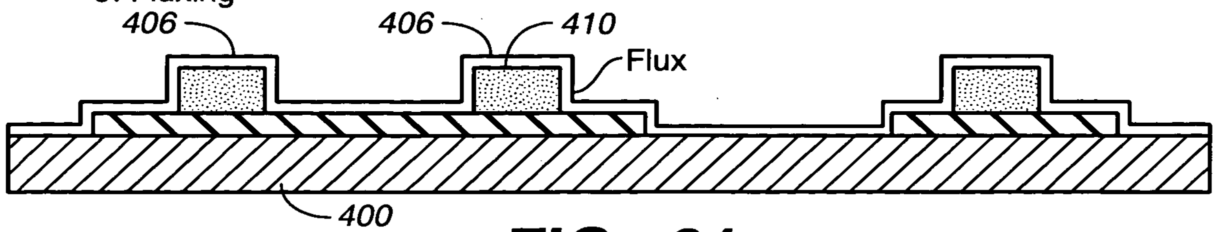


FIG._91

Process Flow of the Resist-free Electroplated Solder Reflow Process

6. Reflow

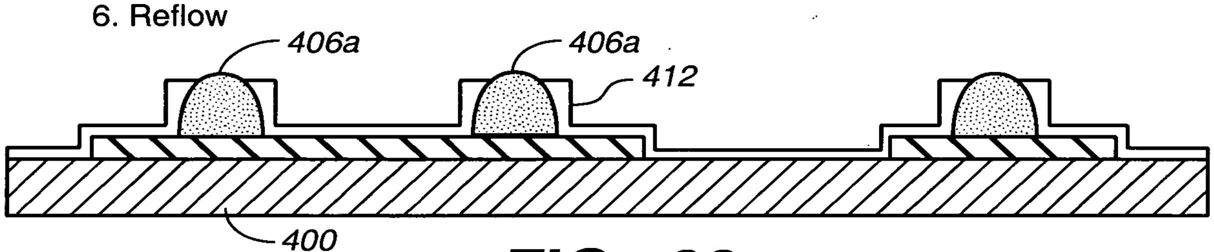


FIG._92

Process Flow of the Resist-free Electroplated Solder Reflow Process

7. Flux Cleaning

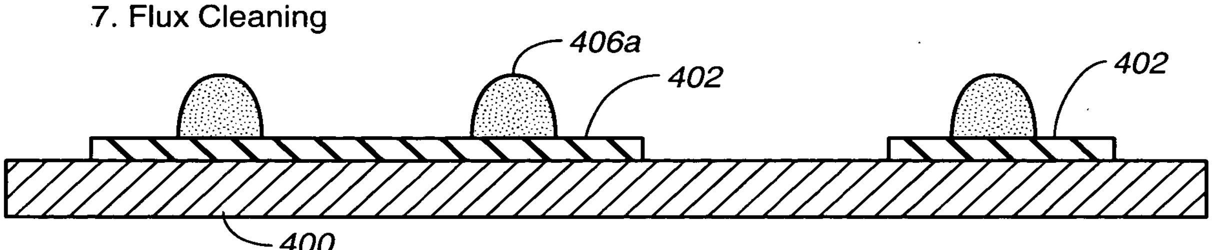


FIG._93

Geometric Dimensions of the Electroplated Bumps

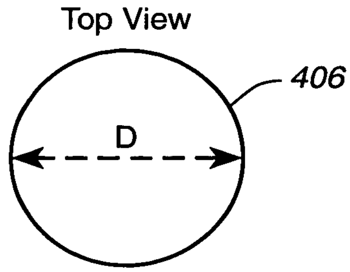


FIG._94

Geometric Dimensions of the Electroplated Bumps

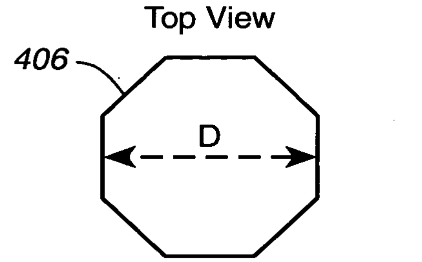


FIG._95

Geometric Dimensions of the Electroplated Bumps

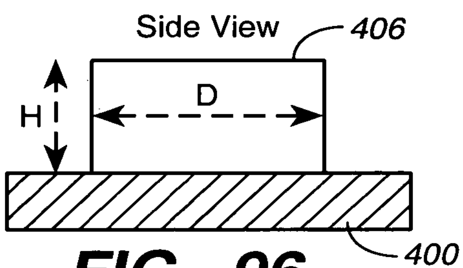


FIG._96

Geometric Dimensions of the Electroplated Bumps

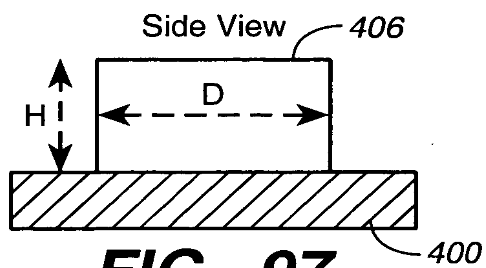


FIG._97

Geometric Shape Change of Electroplated Solder Bumps by Reflow Process

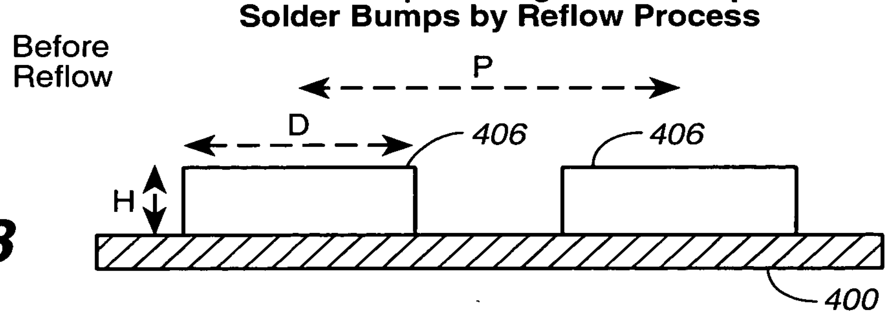


FIG._98

Geometric Shape Change of Electroplated Solder Bumps by Reflow Process

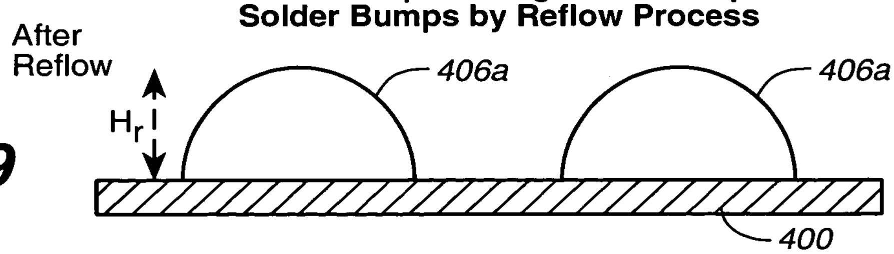


FIG._99

Schematic Drawing of Bridged Bumps

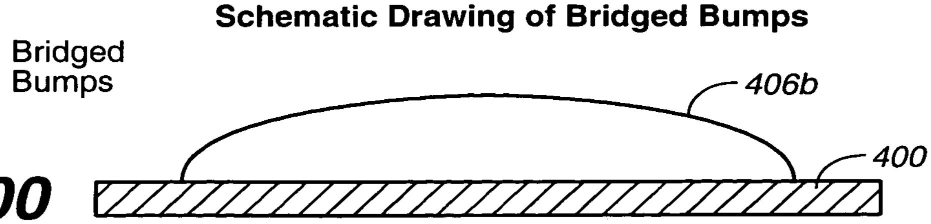


FIG._100

Direct Plating Process

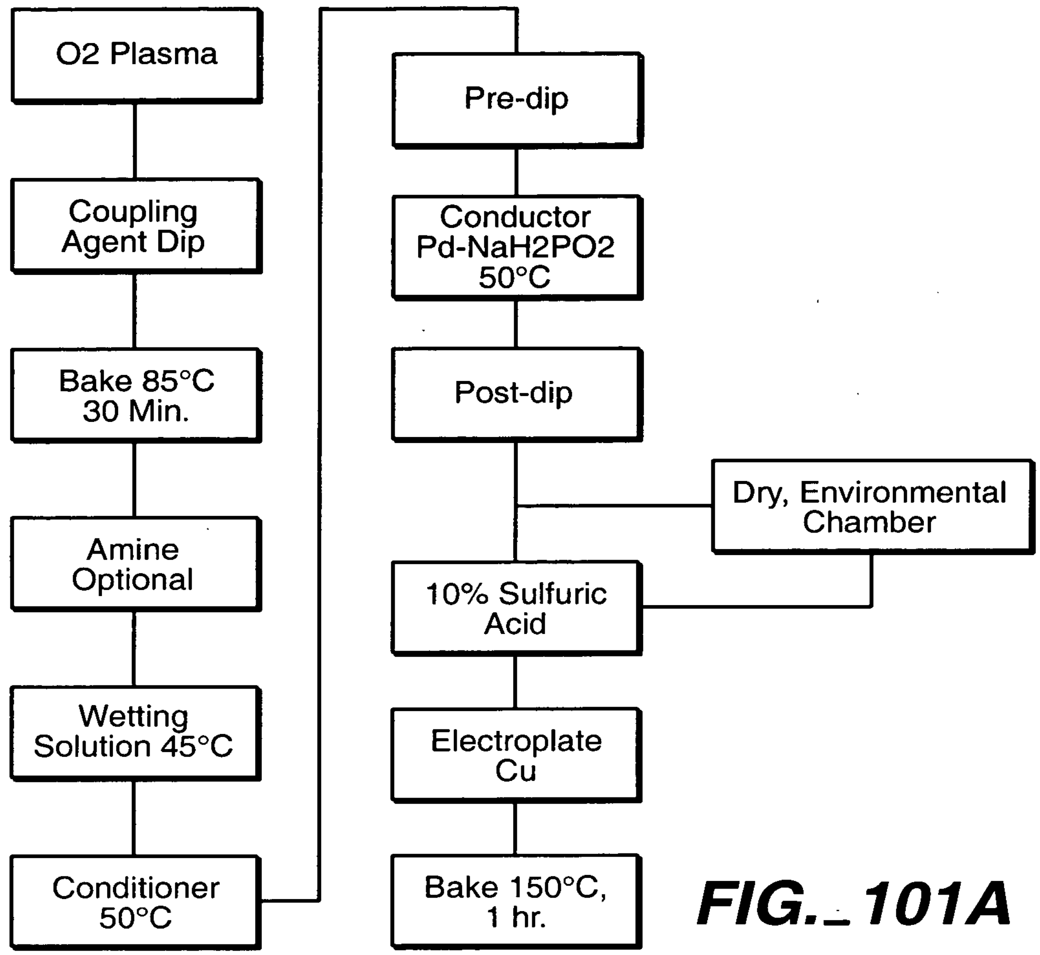


FIG._101A

Stencil Frame Layout

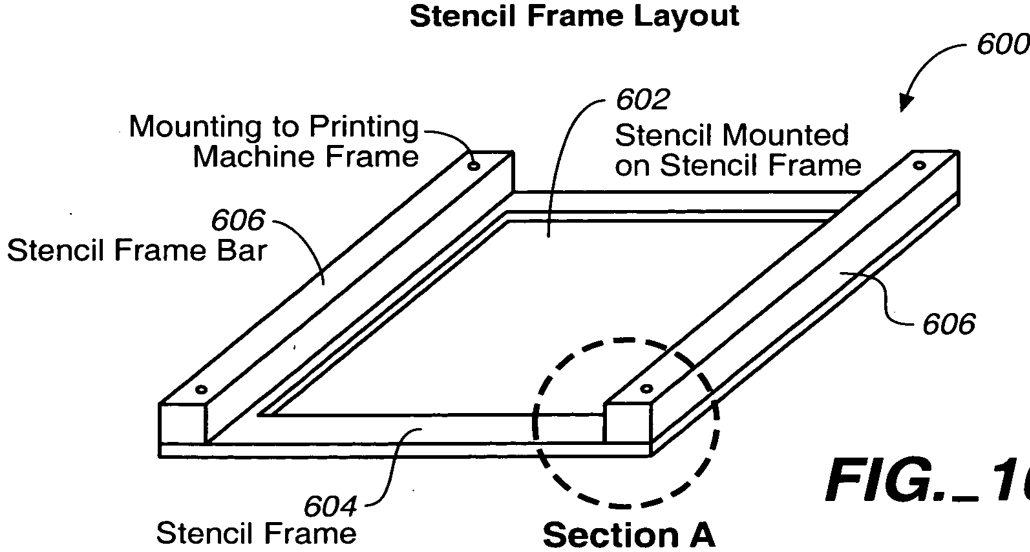
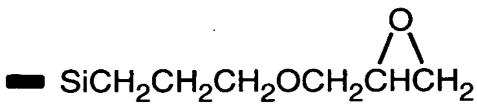
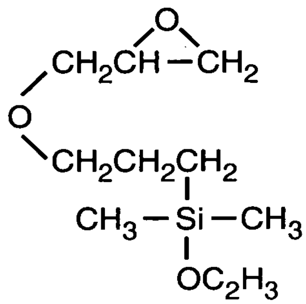
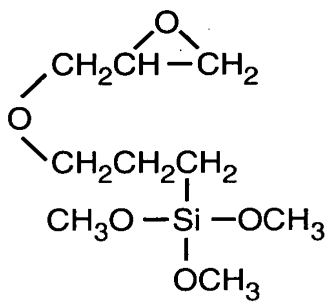


FIG._102

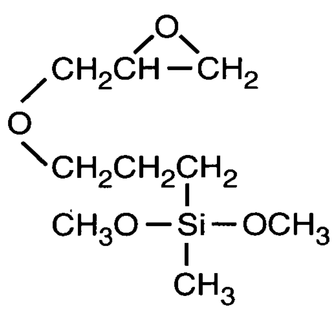




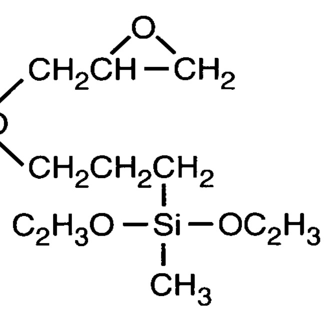
(3-GLYCIDOXYPROPYL)DIMETHYLETHOXY-
SILANE
$C_{10}H_{22}O_3Si$



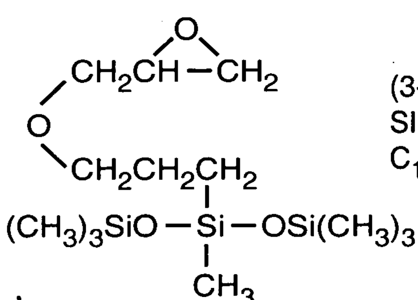
(3-GLYCIDOXYPROPYL)TRIMETHOXYSILANE
3-(2,3-EPOXYPROPOXY)PROPYLTRIMETHOXYSILANE
$C_9H_{20}O_5Si$



(3-GLYCIDOXYPROPYL)METHYLDIMETHOXY-
SILANE
$C_9H_{20}O_4Si$

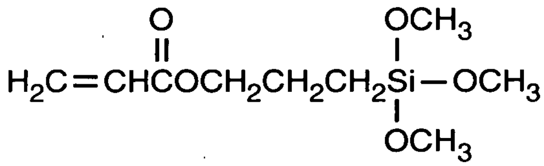


(3-GLYCIDOXYPROPYL)METHYLDIETHOXY-
SILANE
$C_{11}H_{24}O_4Si$



(3-GLYCIDOXYPROPYL)BIS(TRIMETHYL-
SILOXY)METHYLSILANE
$C_{13}H_{32}O_4Si_3$

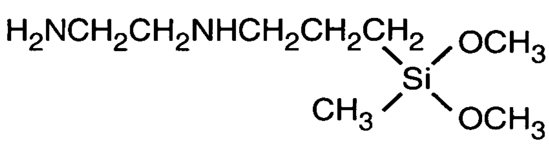
FIG._101B-1



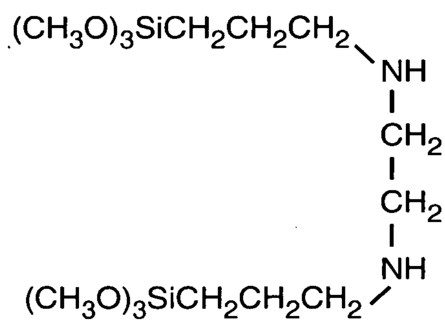
(3-ACRYLOXYPROPYL)TRIMETHOXY-
SILANE, 95%
$C_9H_{18}O_5Si$

$H_2NCH_2CH_2NHCH_2CH_2CH_2Si(OCH_3)_3$

N-(2-AMINOETHYL)-3-AMINOPROPYLTRI-
METHOXYSILANE
$C_8H_{22}N_2O_3Si$



N-(2-AMINOETHYL)-3-AMINOPROPYLMETHYL-
DIMETHOXYSILANE
$C_8H_{22}N_2O_2Si$



BIS(3-TRIMETHOXYSILYL)PROPYL]-
ETHYLENEDIAMINE,
$C_{14}H_{36}N_2O_6Si_2$

FIG._101B-2

Section View of Stencil Frame Components

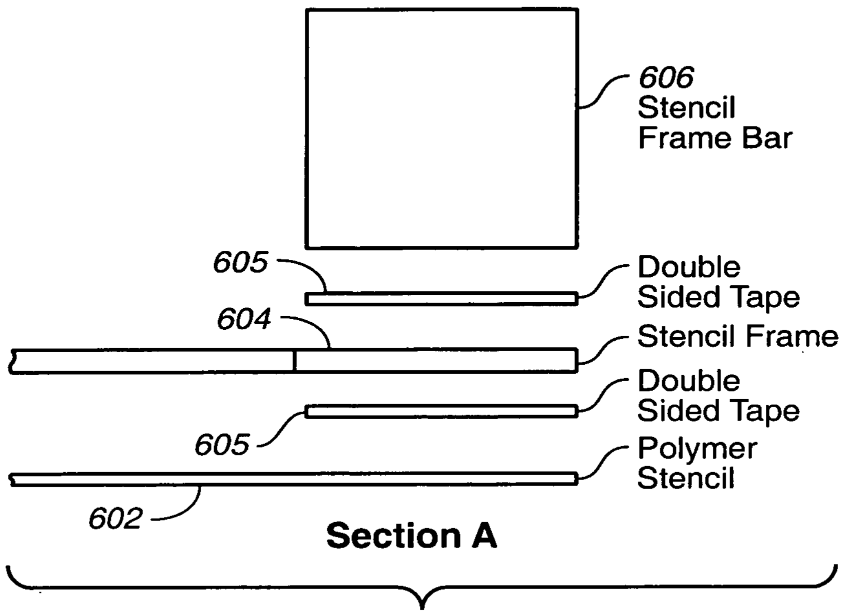


FIG._103

Tapped Hole in Stencil Frame Bar

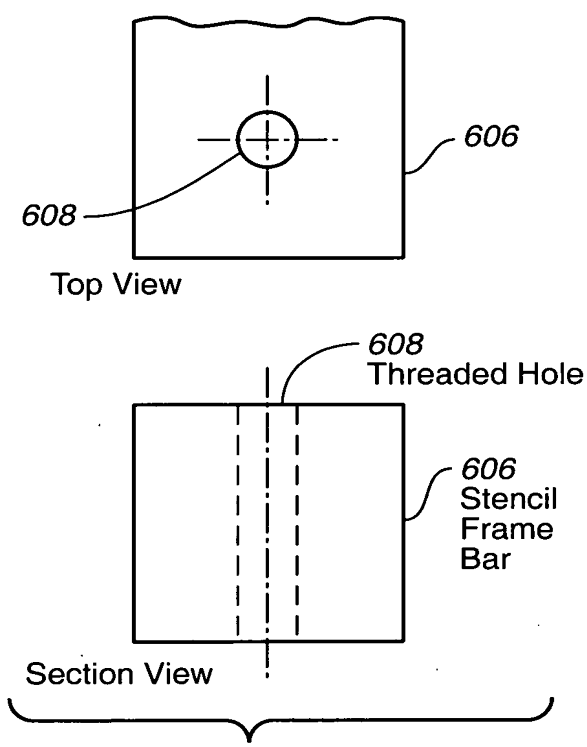


FIG._104

Traditional Joining

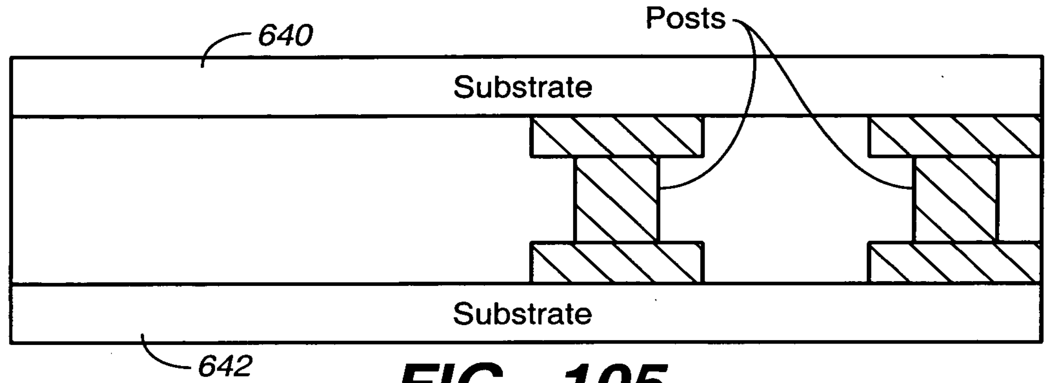


FIG._105

Alignment and Holding Using Long Pin

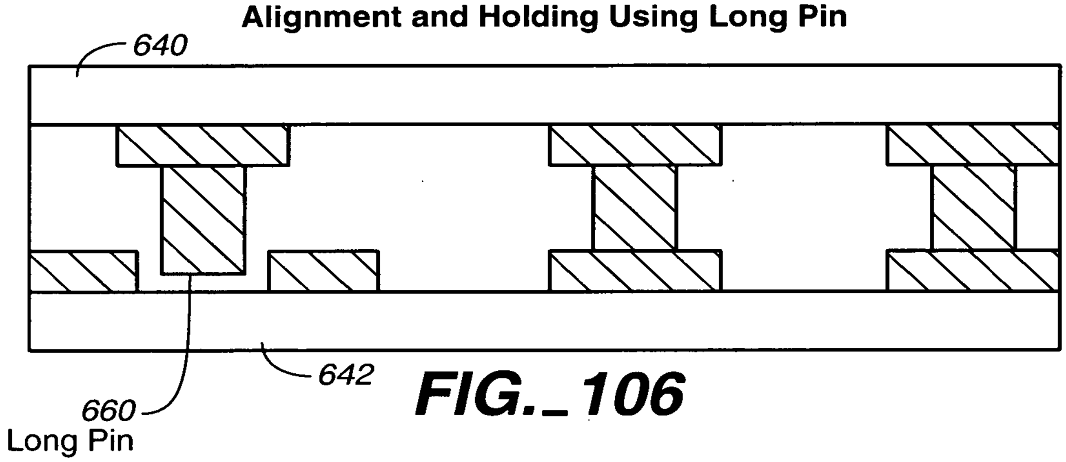


FIG._106

Alignment and Holding Using Thick Pads

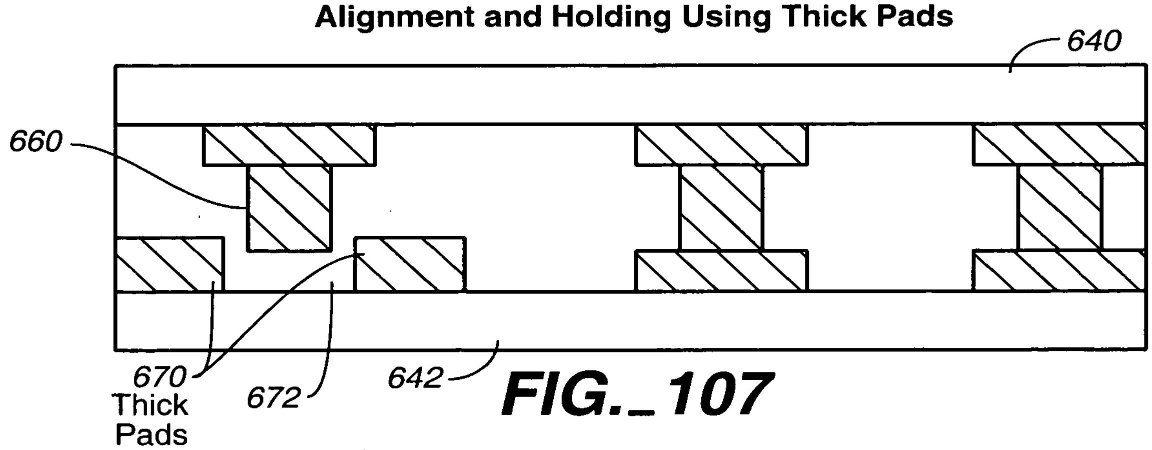


FIG._107

Build-up Process for Long Pin

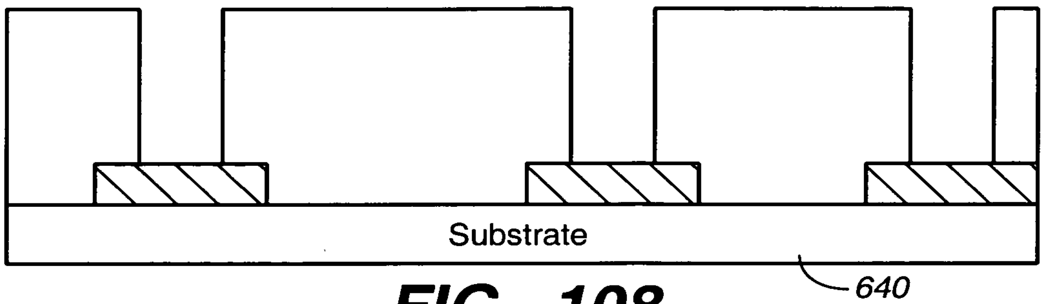


FIG._108

Build-up Process for Long Pin

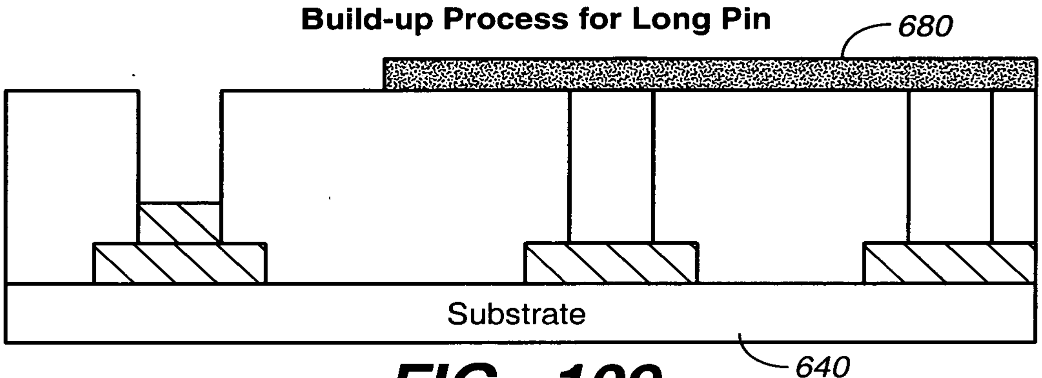


FIG._109

Build-up Process for Long Pin

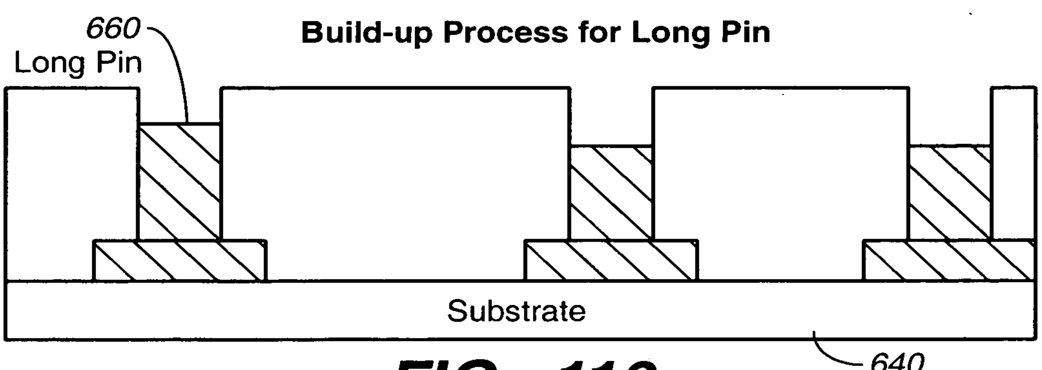


FIG._110

Another Build-up Process for Long Pin

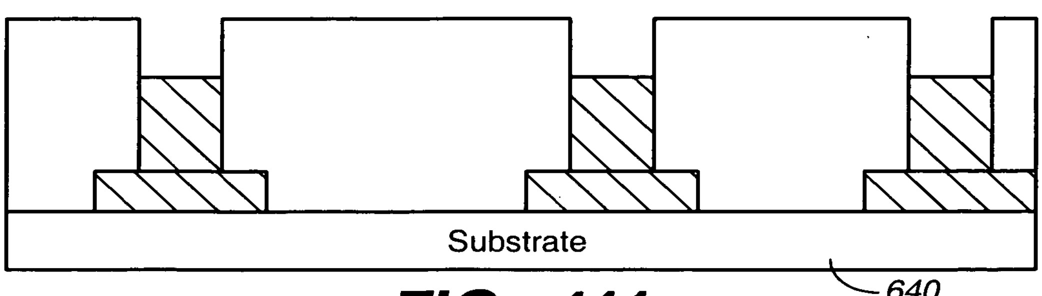


FIG._111

Another Build-up Process for Long Pin

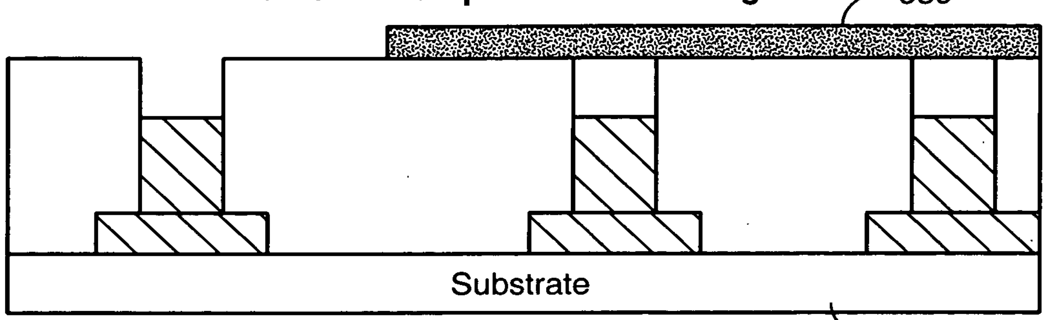


FIG._112

Another Build-up Process for Long Pin

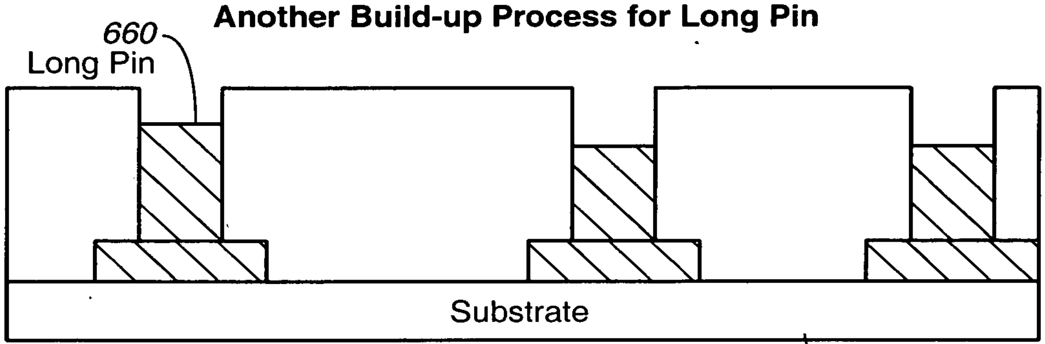


FIG._113

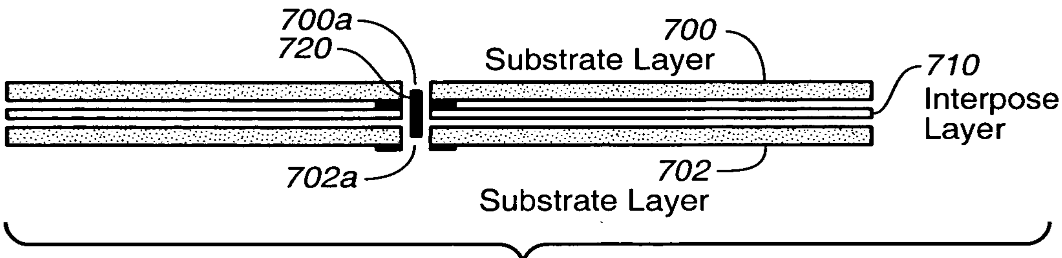


FIG._114

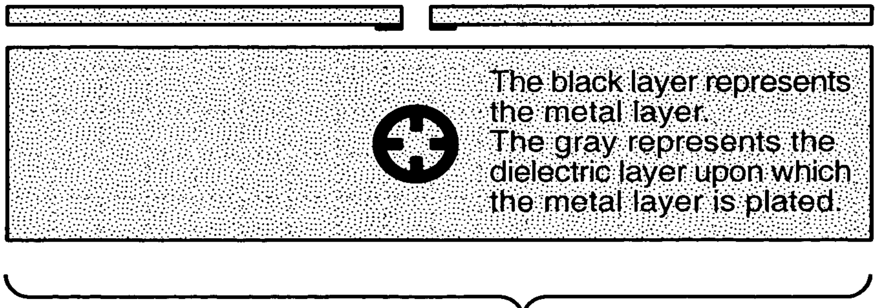


FIG._115

Transient liquid alloy bonding process with separate bonding phases.

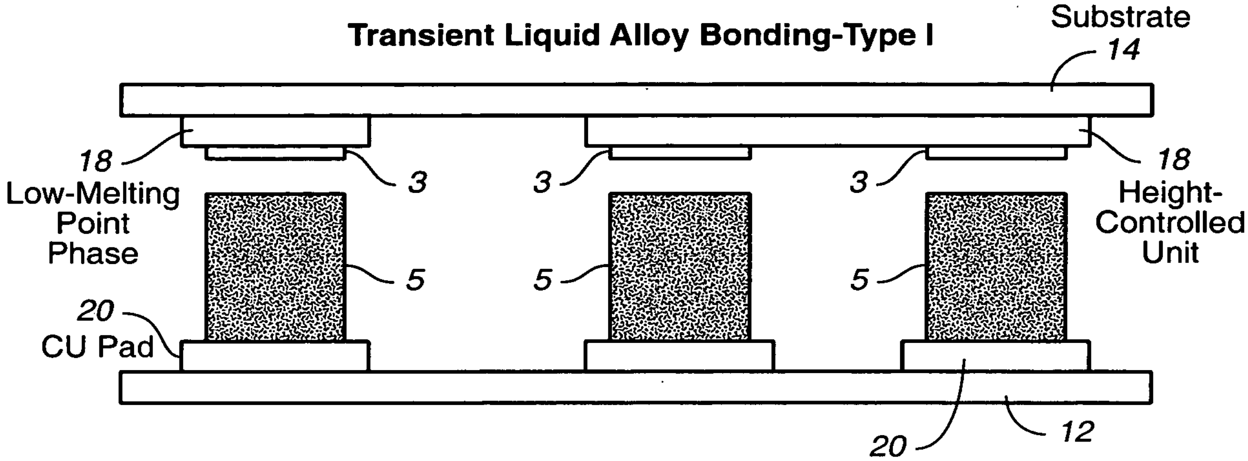


FIG._116

Transient liquid alloy bonding process with one side bonding phases.

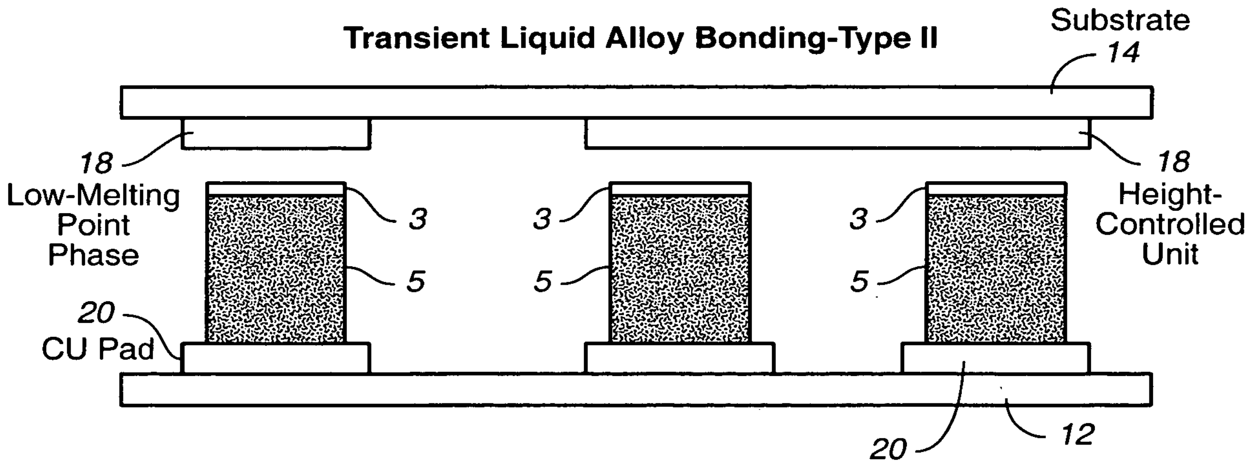


FIG._117

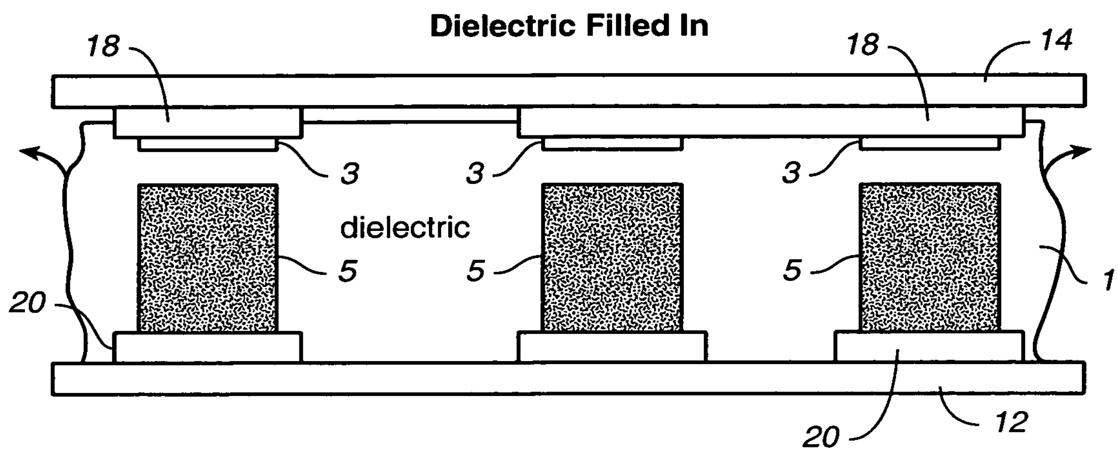


FIG._118

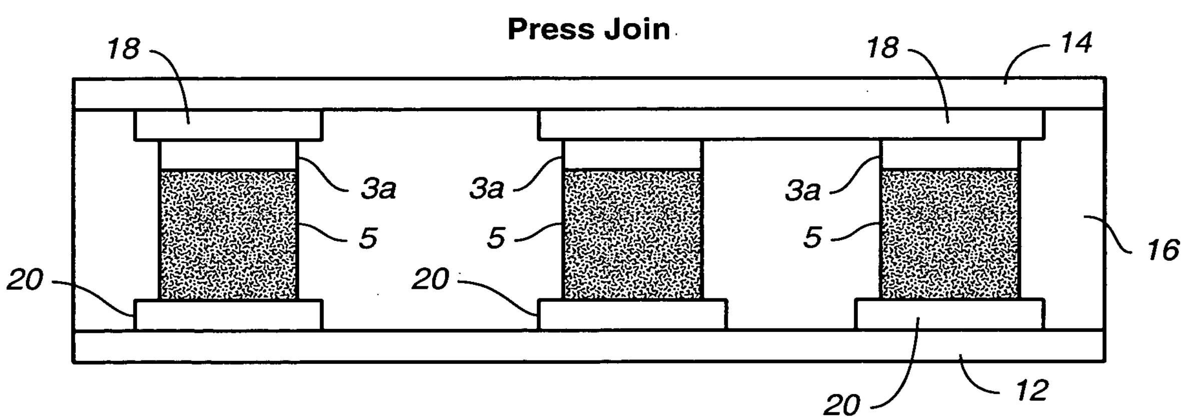


FIG._119

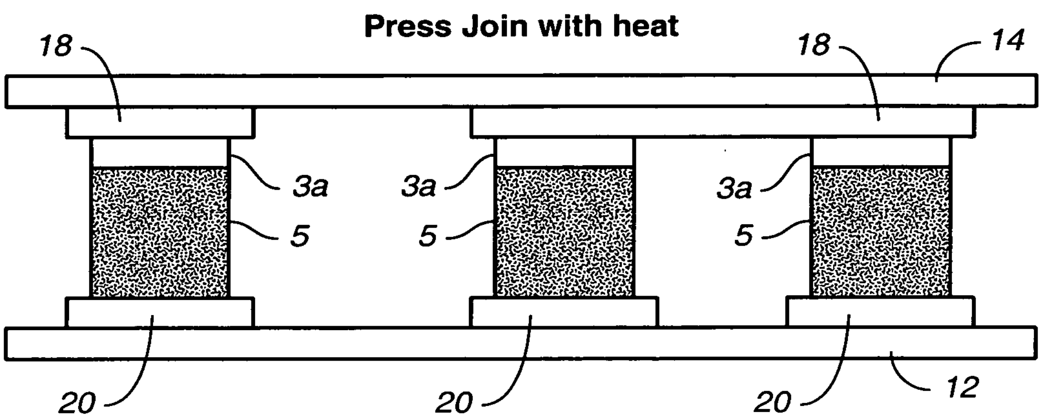


FIG._120

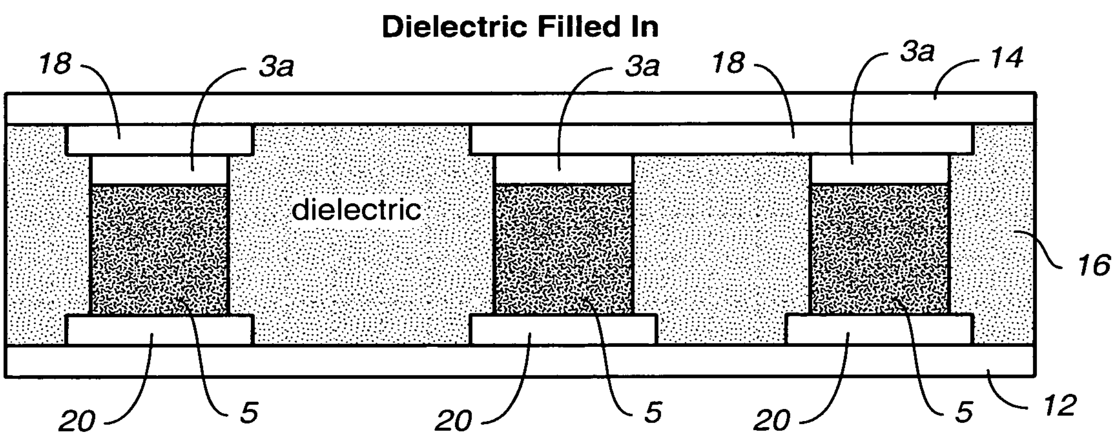


FIG._121

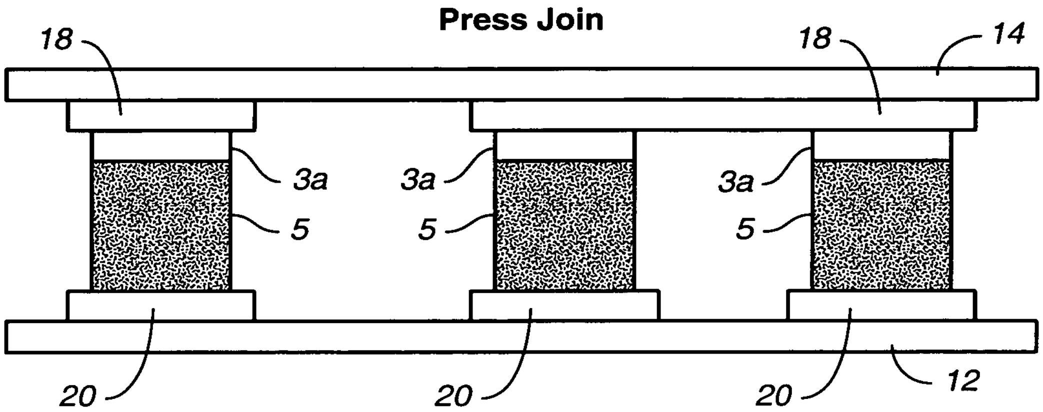


FIG._122

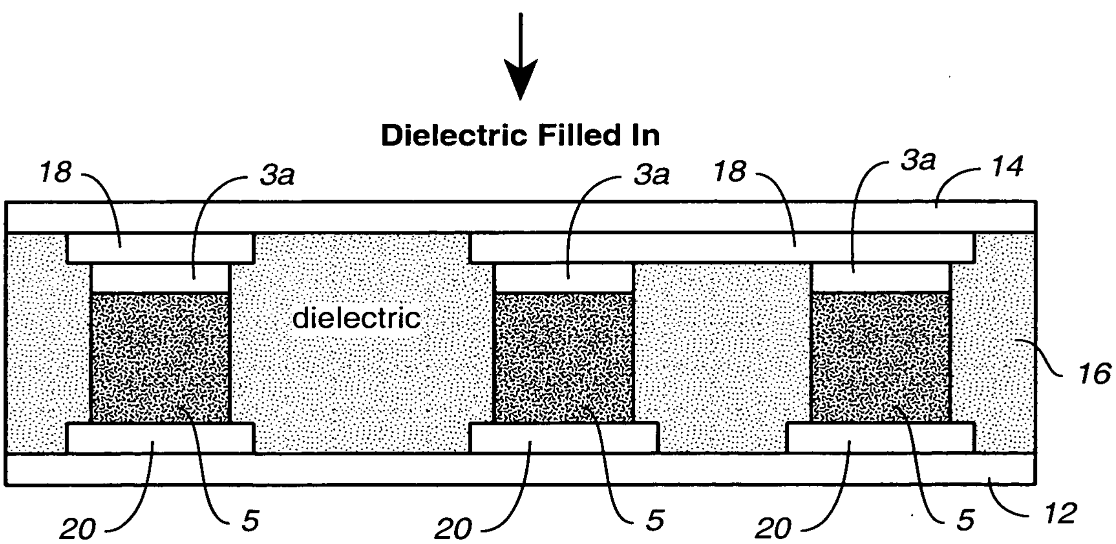


FIG._123

Dielectric Filled In

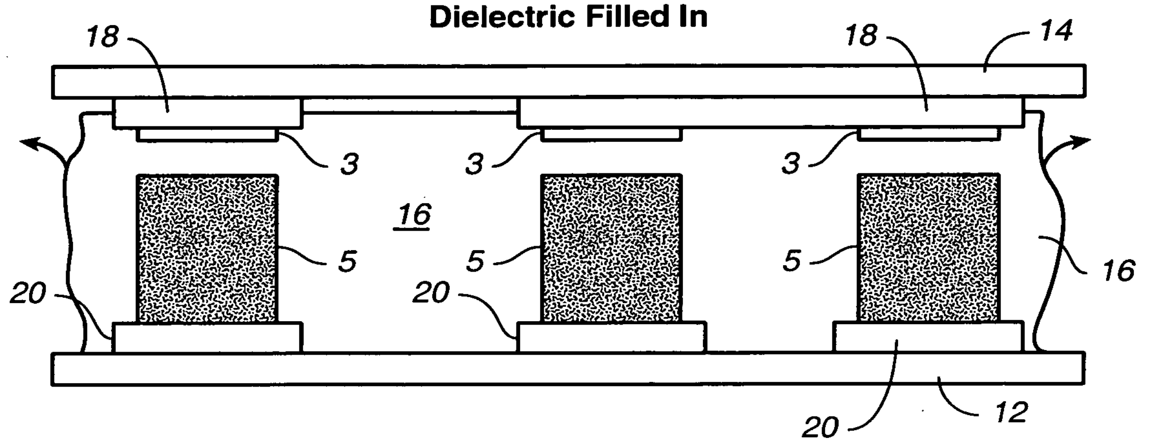


FIG._124

Press Join

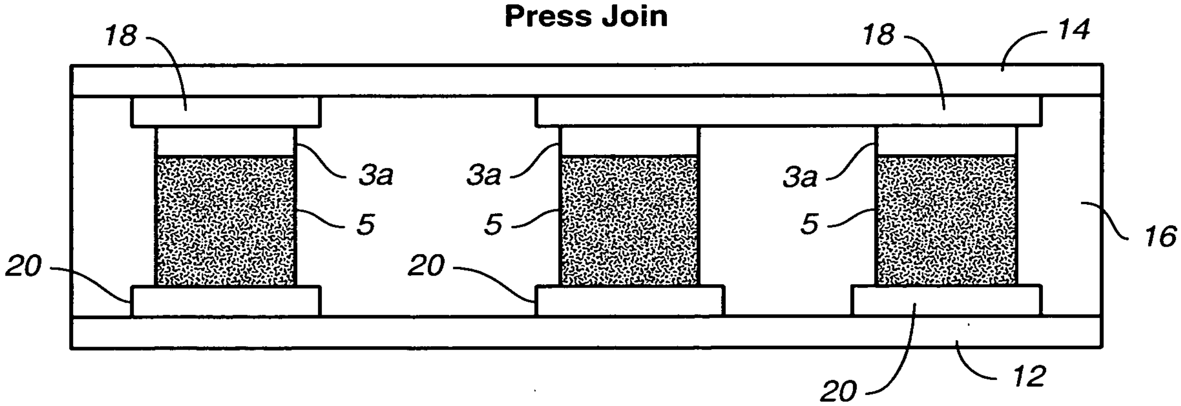


FIG._125